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SK-RF CO.,Ltd

USER MANUAL

SKL3012&SKL3013 Module User Manual

60 GHz one-way high-speed millimeter-wave castellated modules

Document Type	User Manual
Applicable Product	SKL3012 / SKL3013
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Document Summary: Describes host PCB assembly, wiring, mode selection, power-up, data and rotation testing, troubleshooting and maintenance for the SKL3012 transmitter and SKL3013 receiver.

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1 Functional Description

SKL3012 is a wireless transmitter and SKL3013 a wireless receiver. Together, they form a one-way contactless data link. Connect the data source to the SKL3012 TXI differential inputs and the receiving device to the SKL3013 RXO differential outputs. Each host PCB supplies 1.8 V power and mode selection signals. Select the RST connection according to Section 4.2.

The modules support a maximum interface rate of 5.4 Gbit/s and FDR/HDR hardware boot modes, for use in coaxial rotary connectors and high-speed slip-ring data channels.

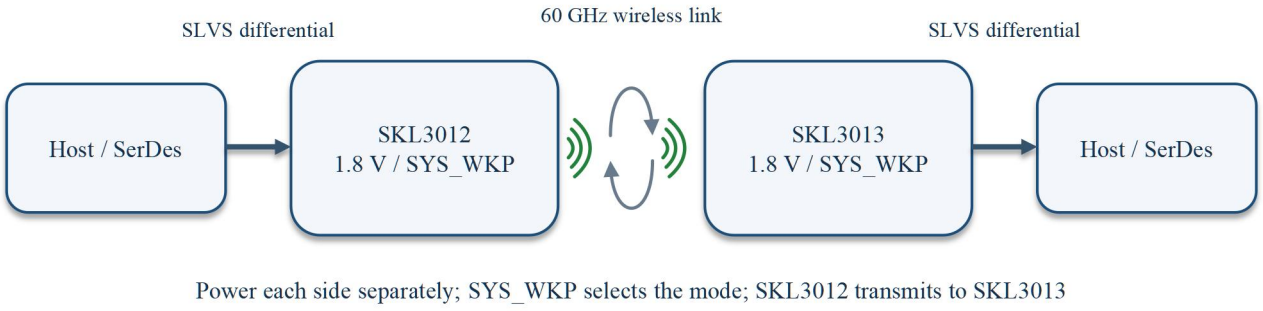


Figure 1. One-way data connection from SKL3012 to SKL3013

2 Pin Definitions

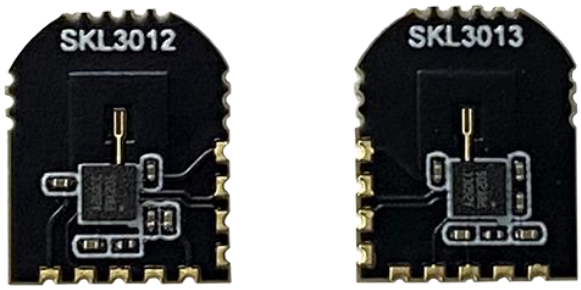


Figure 2. SKL3012 (left) and SKL3013 (right) photographs

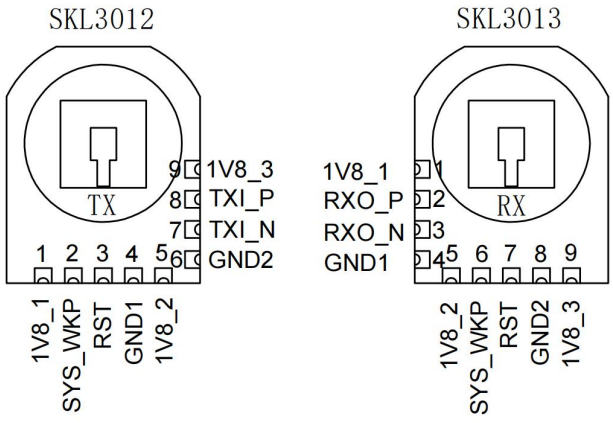


Figure 3. Pin positions and signal names for both models

Table 1. SKL3012 transmitter pin definitions

Pin No.	Signal Name	Description
1	1V8_1	1.8 V power input.
2	SYS_WKP	Boot configuration pin, 1.8 V logic; high selects FDR and low selects HDR.
3	RST	1.8 V active-low reset pin. Outputs the internal power-on delay reset signal, or accepts a low-level reset from host I/O. Leave unconnected when external reset is not required.
4	GND1	Ground.
5	1V8_2	1.8 V power input.
6	GND2	Ground.
7	TXI_N	Transmit differential data input, negative.
8	TXI_P	Transmit differential data input, positive.
9	1V8_3	1.8 V power input.

Table 2. SKL3013 receiver pin definitions

Pin No.	Signal Name	Description
1	1V8_1	1.8 V power input.
2	RXO_P	Receive differential data output, positive.
3	RXO_N	Receive differential data output, negative.
4	GND1	Ground.
5	1V8_2	1.8 V power input.
6	SYS_WKP	Boot configuration pin, 1.8 V logic; high selects FDR and low selects HDR.
7	RST	1.8 V active-low reset pin. Outputs the internal power-on delay reset signal, or accepts a low-level reset from host I/O. Leave unconnected when external reset is not required.
8	GND2	Ground.
9	1V8_3	1.8 V power input.

3 Electrical Characteristics

Table 3. Power supply and temperature parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IN}	Input voltage	1.7	1.8	1.98	V
I_{IN}	Input current (SKL3012/3013)	-	30	-	mA
T_A	Operating ambient temperature	−20	-	+85	°C

Table 4. Digital Interface, SLVS and Carrier Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IH}	Digital control input-high voltage	1.2	1.3	-	V
V_{IL}	Digital control input-low voltage	-	0.5	0.6	V
V_{DIFF_TX}	SLVS transmit-input differential voltage amplitude	100	200	300	mV
V_{CM_TX}	SLVS transmit-input common-mode voltage	160	-	310	mV
Z_{DIFF_TX}	SLVS transmit input differential impedance	-	100	-	Ω
V_{DIFF_RX}	SLVS receive-output differential voltage amplitude	80	200	300	mV
V_{CM_RX}	SLVS receive-output common-mode voltage	80	200	300	mV
Z_{DIFF_RX}	SLVS receive output differential impedance	-	100	-	Ω
F_{OSC}	Carrier frequency	-	60.6	-	GHz

4 Reference Design

4.1 Peripheral Reference Circuit and Pin Connections

Table 5. Power supply and control wiring

Signal	SKL3012 pin	SKL3013 pin	Connection
1V8	1 / 5 / 9	1 / 5 / 9	Connect all three supply pins to 1.8 V
GND	4 / 6	4 / 8	Connect to common host-board ground
RST	3	7	For reset connections, see Section 4.2.
SYS_WKP	2	6	1.8 V boot selection; high=FDR, low=HDR

The recommended input range is 1.7–1.98 V, typically 1.8 V. The reference circuit uses 0.1 µF decoupling near the supply pins, and 1 kΩ resistors for the illustrated RST and FDR boot pull-ups. For the actual RST connection, see Section 4.2.

Table 6. Differential data wiring

Module	Pin No.	Signal	Connection
SKL3012	8 / 7	TXI_P / TXI_N	Connect to the positive and negative transmit terminals of the host data source
SKL3013	2 / 3	RXO_P / RXO_N	Connect to the positive and negative terminals of the data-receiving device

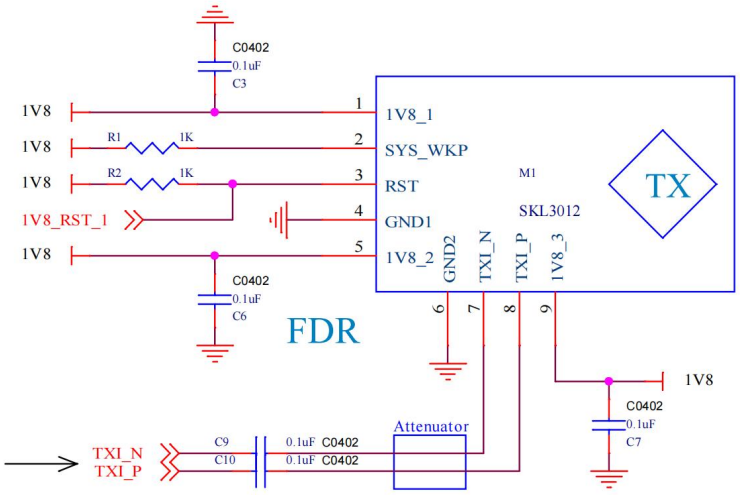


Figure 4. SKL3012 transmitter FDR reference circuit

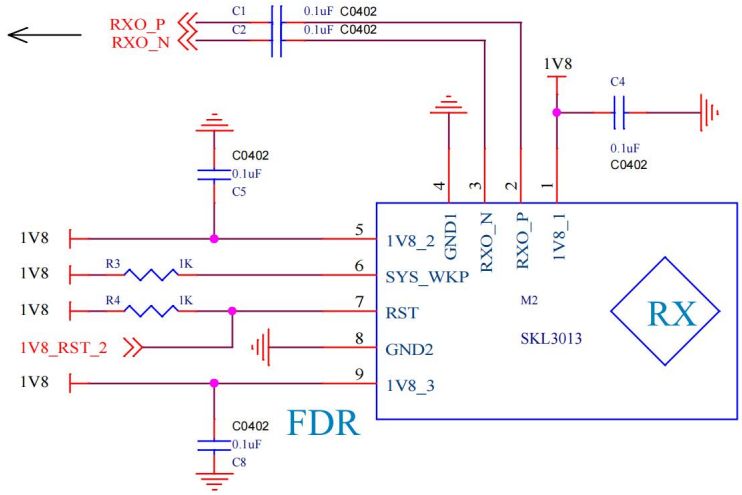


Figure 5. SKL3013 receiver FDR reference circuit

Route differential pairs with correct P/N polarity, continuous and symmetrical traces. Place RXO output AC-coupling capacitors close to the module and TXI input capacitors close to the host. The illustrated AC-coupling capacitors are all 0.1 μF, 0402.

4.2 Reset Interface

SKL3012 and SKL3013 have internal power-on delay reset circuits. RST uses 1.8 V logic and is active low. Select one of the following connections.

(1) Synchronous reset of external devices. Connect RST to a level-compatible active-low reset input, such as an Ethernet PHY reset pin. At power-up, the module outputs its internal delayed reset signal through RST to reset the external device synchronously with the module's ST60A2.

(2) Host-controlled reset. Connect RST to level-compatible host I/O. Pull it low to reset, then release it to high impedance. An open-drain host output can avoid actively driving high while the module outputs a reset-low signal.

(3) Independent power-up. When neither synchronous external reset nor host control is required, leave RST unconnected. The internal circuit performs the module's power-on reset.

4.3 TXI Attenuation and AC Coupling

SKL3012 TXI receives SLVS differential signals from the host. If the host output amplitude is too high, an attenuation network can bring the input amplitude at the module into the recommended range.

Measure P−N differential peak-to-peak voltage at the module TXI input using the actual termination, operating rate and host output setting. The recommended input is 200–600 mVpp, equivalent to 100–300 mV differential amplitude. Within this range, use the reference connection directly. Above the upper limit, first reduce the host output setting; add attenuation if it remains excessive. Below the lower limit, check the host output setting and interconnect loss.

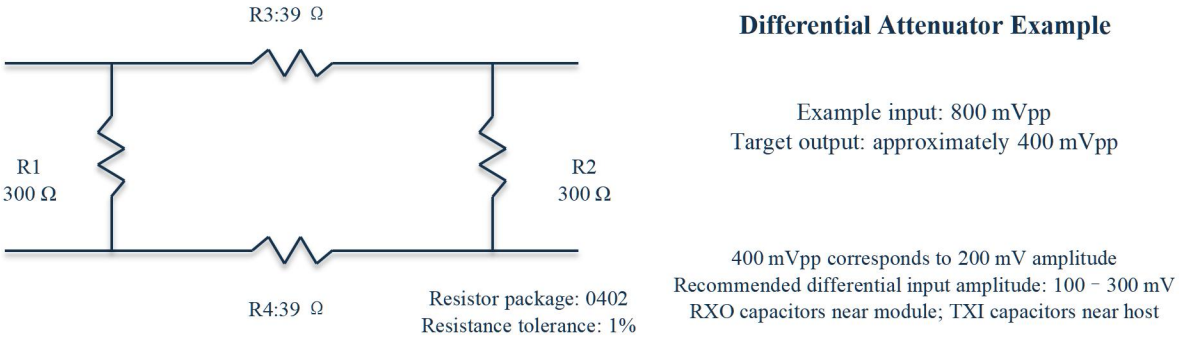


Figure 6. Differential input attenuation and AC-coupling example

Use Figure 6. Insert 39 Ω in series with each P and N line, and connect 300 Ω across P/N at both ends of the network. Use 0402, 1% resistors and a symmetrical layout. Place TXI AC-coupling capacitors near the host, following this model's reference circuit.

The illustrated reduction from 800 mVpp to approximately 400 mVpp is a component-selection example. After assembly, remeasure differential peak-to-peak and common-mode voltages at TXI and verify data transfer. Check this model's electrical table and adjust resistance for the actual source impedance, termination and measurements.

With an 800 mV differential peak-to-peak host output, the illustrated 39 Ω series and 300 Ω shunt resistor network adjusts the input to approximately 400 mV peak-to-peak, equivalent to a 200 mV differential amplitude. Resistor tolerance is 1%.

The recommended SKL3012 input differential amplitude is 100–300 mV and common-mode voltage is 160–310 mV. The SKL3013 receive outputs use 100 Ω differential termination, with a typical output amplitude of 200 mV. Measure the difference between P and N; its peak-to-peak value is twice its amplitude.

4.4 8b/10b Data Encoding

Use 8b/10b encoding on the SLVS differential interface at line rates above 100 Mbit/s. Encoding is performed by the transmitting host, FPGA or SerDes, with corresponding decoding at the receiving host; the module carries the encoded serial signal. LDR single-ended data and differential data at or below 100 Mbit/s operate in their corresponding modes.

8b/10b maps each 8-bit data byte to a 10-bit line code group. The encoder selects valid codewords according to running disparity, maintaining DC balance and limiting consecutive identical bits to five. Sufficient transitions support receiver decisions and host clock recovery, avoiding errors caused by long runs of zeros, ones or biased data.

Use valid D code groups for data bytes and protocol-defined valid K code groups where control characters are required. The receiver checks code-group validity, running disparity and character boundaries before recovering payload data. During idle periods, send valid, DC-balanced encoded sequences and keep encoding rules consistent at both ends.

Line rate includes encoding overhead. For example, a 5 Gbit/s line provides at most 4 Gbit/s for 8b/10b data fields, before preamble, idle-character and protocol overhead. Record line rate and effective payload rate separately in host settings and test records.

64b/66b relies on scrambling for statistical DC balance and cannot directly replace the 8b/10b format required here. If the existing bus uses another encoding, adapt the format in the host or bridge logic before feeding the module's differential input.

4.5 Preamble and Burst-Data Timing

At the start of high-speed transmission, the receiver's adaptive decision threshold requires settling time. Send a continuous, DC-balanced, 8b/10b-encoded preamble before the payload, and start the application frame only after receiver decisions have stabilized. The preamble establishes the link and is not payload.

Preamble duration must cover receiver settling and code-group synchronization, with timing margin. Transmit the complete preamble before valid data begins.

Convert preamble duration to bits using the line rate: $N = \text{ceil}(R \times t_{HEADER})$. R is in bit/s and t_{HEADER} is in seconds; round up to complete 10-bit code groups. At 5 Gbit/s, 50 ns and 90 ns correspond to 250 and 450 bits. At 500 Mbit/s, they correspond to 25 and 45 bits; send at least 30 and 50 bits respectively to complete the code groups.

Choose valid 8b/10b idle or training code groups allowed by the associated protocol, maintaining continuous running disparity. The illustrated alternating 0/1 sequence explains threshold settling; actual transmission must still use valid code groups and meet receive-character alignment requirements.

If transmission stops for longer than the selected t_{HEADER}, send the complete preamble again before the next transfer. In half-duplex operation, first switch the direction at both ends and allow device states to settle, then send the preamble and finally the payload. Meet direction-switching and preamble timing separately.

The receiving host accepts application data after the preamble ends and code-group/frame boundaries are confirmed. Test initial startup, restart after long idle, direction changes, different rates and the actual assembly gap. Record discarded training data, code-group errors, disparity errors and payload verification results separately.

5 Mode Configuration

5.1 Boot Configuration

Table 7. Boot modes and rates

SYS_WKP	Control Mode	Data Rate Mode	Interface rate range
1	HW-forced	FDR-DIFF	1 Mbit/s～5 Gbit/s
0	HW-forced	HDR-DIFF	500 Mbit/s～5.4 Gbit/s

(1) FDR-DIFF: SYS_WKP=1 selects forced hardware configuration; the interface rate is 1 Mbit/s–5 Gbit/s.

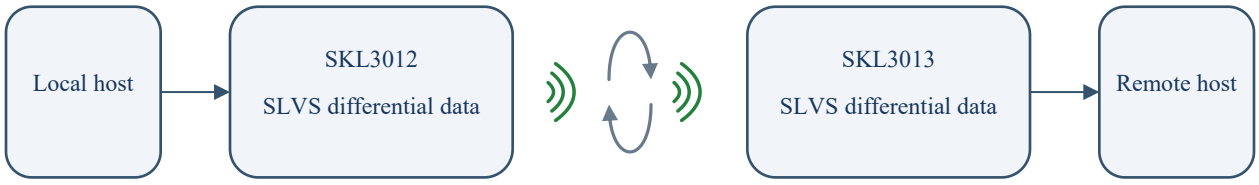
(2) HDR-DIFF: SYS_WKP=0 selects forced hardware configuration; the interface rate is 500 Mbit/s–5.4 Gbit/s.

Standard products select FDR/HDR through SYS_WKP; I2C is used for internal configuration. Set SYS_WKP on both sides before power-up and match the modes and interface rates.

5.2 FDR Mode Connections

SYS_WKP=1 selects FDR. Configure the SKL3012 transmitter and SKL3013 receiver separately, keeping the data mode and interface rate the same.

FDR boot connection: SYS_WKP=1 at both transmitter and receiver



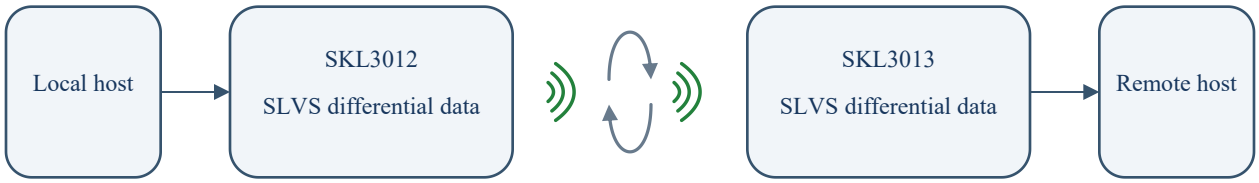
One-way transmission: left module transmits, right module receives

Figure 7. SKL3012&SKL3013 FDR mode communication and boot connections

5.3 HDR Mode Connections

SYS_WKP=0 selects HDR. Configure the SKL3012 transmitter and SKL3013 receiver separately, keeping the data mode and interface rate the same.

HDR boot connection: SYS_WKP=0 at both transmitter and receiver



One-way transmission: left module transmits, right module receives

Figure 8. SKL3012&SKL3013 HDR mode communication and boot connections

6 Communication Connections

Connect the data source to the transmitting module and the receiving host to the receiving module. Power each side separately. Module data direction is fixed; use the transmitter and receiver models as a pair.

FDR boot connection: SYS_WKP=1 at both transmitter and receiver



One-way transmission: left module transmits, right module receives

Figure 9. SKL3012&SKL3013 communication connections

7 Assembly Instructions

7.1 Soldering and Installation Preparation

(1) Confirm SKL3012 as the transmitter and SKL3013 as the receiver. Check that the antennas, PCBs and pads are intact.

(2) Create host PCB pads and cutouts using the corresponding model's dimension drawing. Check all nine pins and the data direction.

(3) Solder the modules with the antenna faces up. Check solder joints and ensure that supply, ground and adjacent pads are not shorted.

(4) Secure the host PCBs and cables to keep the modules stable during equipment movement.

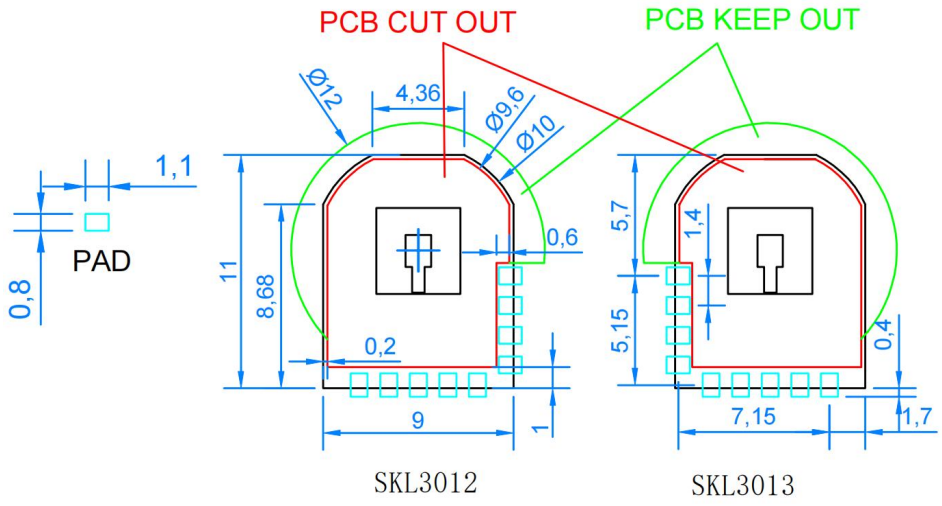


Figure 10. SKL3012 and SKL3013 cutout, pad and keep-out dimensions (unit: mm)

SKL3012 is shown on the left and SKL3013 on the right; the pads are 1.1 mm × 0.8 mm. Lay out each host PCB according to its P1 orientation, red cutout and green keep-out area.

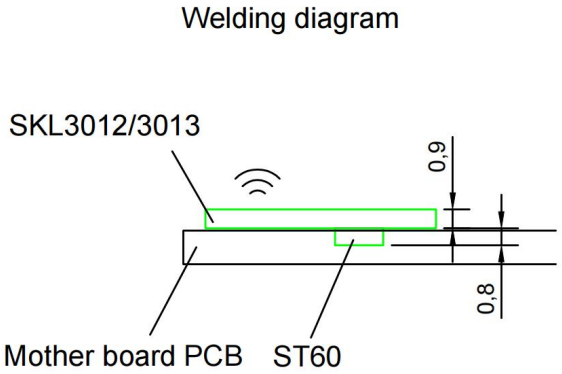


Figure 11. Module-to-host-PCB soldering cross-section (unit: mm)

7.2 Paired Assembly and Antenna Alignment

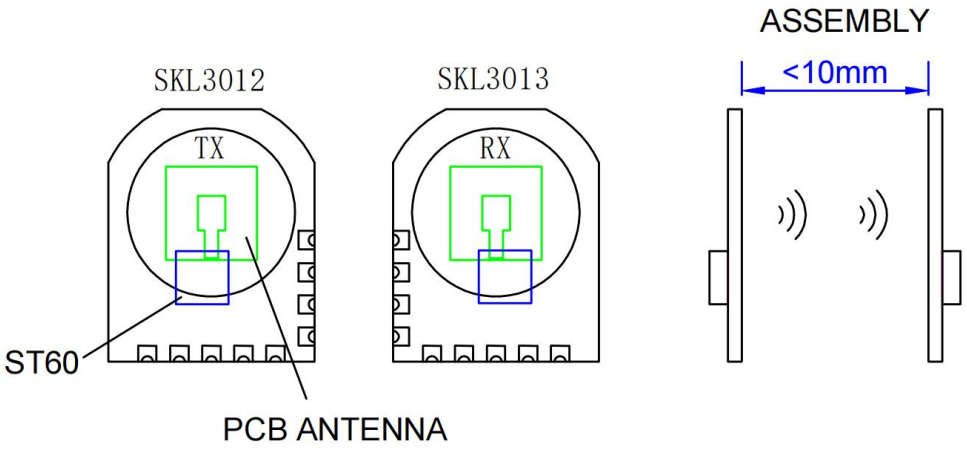


Figure 12. Paired assembly and antenna spacing

(1) Position the PCB patch antenna faces opposite each other and align them coaxially. Use approximately 5 mm spacing for initial commissioning and keep it below 10 mm.

(2) Remove metal parts, screws, metallic paint and other reflective objects from the millimeter-wave path. Provide a nonmetallic window in front of the antennas when using a metal enclosure.

(3) With power disconnected, check the full movement travel for collisions, module displacement and cable strain.

(4) Secure the assembly position. After assembly, follow Section 9 to verify communication while stationary and moving.

Paired operation: SKL3012 transmits, SKL3013 receives.

Assembly spacing: below 10 mm; approximately 5 mm recommended.

8 Power-Up and Operation

8.1 Initial Power-Up

(1) With power disconnected, recheck both model numbers, 1V8/GND, RST and data P/N wiring.

(2) Secure the antennas at approximately 5 mm spacing and set SYS_WKP boot levels on both sides.

(3) Apply the 1.8 V supply separately to each side. If using host-controlled reset, follow Section 4.2.

(4) Wait for the internal power-on reset to release. If the host additionally holds RST low, release the host I/O after the supply is stable and boot configuration is ready.

(5) Start the data source, transmit known data from SKL3012 to SKL3013 and check the received result.

Before power-up, check differential input levels as described in Section 4.3. Reset connections and timing are described in Section 4.2.

9 Data Tests

9.1 Data-Transmission Tests

(1) At fixed spacing, perform one-way transmission using a fixed data pattern or actual application data.

(2) Compare the amount sent by the source with the amount received by the receiving device. Save error statistics.

(3) Increase the rate progressively to the target value. After each adjustment, check the modes, electrical amplitude and received results at both ends.

(4) Perform a wired or board-level comparison using the same data source, receiving device and data pattern.

(5) Save the mode, interface rate, total data quantity, error count and duration.

For bit-error testing, record transmitted and erroneous bit counts. For packet applications, record packet lengths, counts, loss and checksum errors.

9.2 Assembly and Rotation Tests

(1) Once stationary communication is normal, keep data transmission continuous and start the rotary mechanism.

(2) Check received data at the required system speed and throughout the full travel, observing antenna coaxial alignment and spacing changes.

(3) Fit the actual enclosure and repeat the test with the final window material, thickness and mounting structure.

(4) Run continuously at the actual operating temperature, recording supply, temperature, assembly spacing and data statistics.

(5) If communication fails, stop rotation and check the stationary link first, then vary assembly and interface conditions separately for comparison.

10 Common Questions and Operating Checks

10.1 Common Questions and Corrective Actions

Table 8. Troubleshooting

Symptom	Checks and Corrective Action
No data	Check model numbers and direction: the data source connects to SKL3012 and the receiver to SKL3013. Check supply, ground and RST.
Data errors or failure to synchronize	Check SYS_WKP on both sides, interface rate, P/N polarity and host initialization.
More errors at high rates	Check input amplitude, common-mode voltage, 100 Ω receive termination, coupling capacitors and differential traces.
Unstable communication during movement	Check spacing below 10 mm, coaxial alignment, module fixing, cable strain and metal obstructions.

(1) Disconnect power and stop rotation before soldering, wiring or mechanical adjustments. Take ESD precautions. After maintenance, start according to Section 5, then follow Section 9.

10.2 Technical Support

When contacting technical support, provide the product model and revision, connections and settings at both ends, power-supply conditions, indicator states, symptoms and steps to reproduce the issue. Include wiring and assembly photographs, test settings and recorded results.

11 Revision History

Date	Revision	Description of Changes
2026-11-04	V1.0	(1) Prepared the English user manual from the reviewed Chinese edition, organizing pin definitions, electrical characteristics, reference design and operation around the actual one-way transmitter/receiver connections. (2) Added photographs and complete pin tables for both models; described SYS_WKP selection of FDR/HDR and interface-rate matching at both ends. (3) Described RST connections for synchronous reset, host pull-low control and floating operation; organized transmitter TXI attenuation, AC coupling and separately displayed transmitter/receiver reference circuits. (4) Added 8b/10b encoding, preamble timing, power-up checks, data and rotary assembly tests, and troubleshooting. (5) Updated one-way connection diagrams with same-direction three-arc wireless symbols on both sides of the rotation symbol; standardized matching frames and explanatory-text spacing; completed captions and internal references. (6) Standardized the bootstrap configuration table widths and layout using the SKA2Dxx user manual, retaining configuration values, pin aliases, font sizes, minimum row heights and cell margins. (7) Equalized the Min., Typ. and Max. columns in parameter tables, retaining all values, conditions, units, font sizes and standard line spacing. (8) Checked the destinations of contents entries and section, figure and table references; rebuilt Word/WPS-compatible internal bookmark links and corrected misplaced or invalid targets. (9) Standardized chapter names, order and content allocation using the common outline, retaining technical descriptions and illustrations; updated the contents, figure/table numbering and internal references. Moved initial power-up under Power-Up and Operation, standardized Common Questions and Operating Checks, and added the information required for technical support. (10) Prepared and checked this English edition against the current Chinese edition, preserving numbered items, parameters, illustrations, commands and operating instructions.