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SK-RF CO.,Ltd

DATASHEET

SKL3012&SKL3013 Module Datasheet

60 GHz one-way high-speed millimeter-wave castellated modules

Document Type	Product Datasheet
Applicable Product	SKL3012 / SKL3013
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Document Summary: Describes the differential data interfaces, power supply, FDR/HDR modes, reference circuits and assembly requirements of the SKL3012 transmitter and SKL3013 receiver for hardware selection and mechanical integration.

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1 Product Overview

The SKL3012 and SKL3013 are 60 GHz RF modules built around the ST60A2 millimeter-wave transceiver, with integrated PCB patch antennas and castellated pads for direct mounting to the host PCB. The SKL3012 converts differential host input data to millimeter-wave signals for transmission; the SKL3013 converts received millimeter-wave signals to differential output data. Together, they form a unidirectional high-speed contactless data link.

2 Features

- 60 GHz V-band communication with integrated PCB patch antennas.
- Maximum interface rate: 5.4 Gbit/s. The applicable FDR and HDR rate ranges are listed separately.
- SKL3012 transmits and SKL3013 receives; used as a pair for one-way communication.
- Supports coaxial high-speed rotation for contactless rotary connectors and high-speed data channels in slip rings.
- Castellated assembly; recommended face-to-face antenna spacing approximately 5 mm, with assembly drawing requirements below 10 mm.

3 Applications

- Contactless high-speed rotary connectors
- High-speed data channels in slip rings.

4 Block Diagram and Appearance

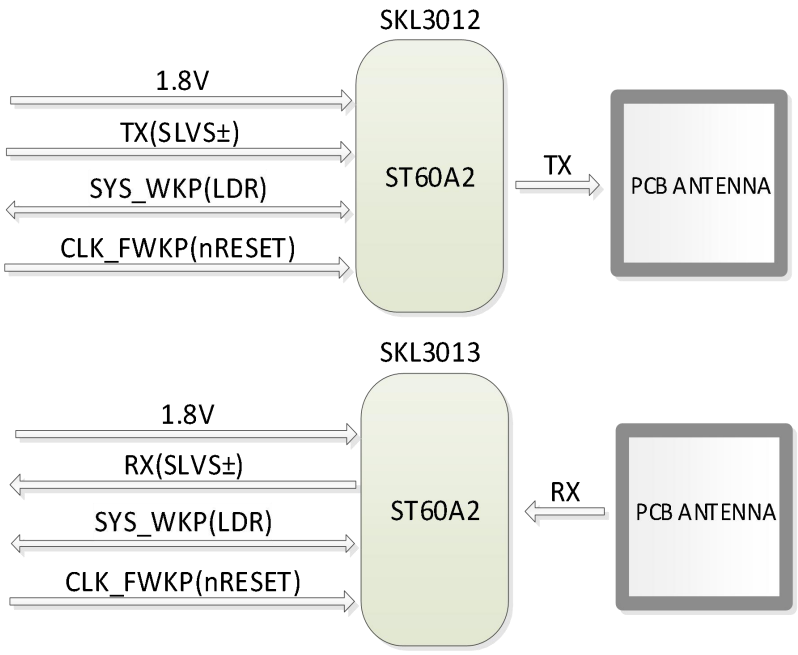

Figure 1. Functional block diagrams of the SKL3012 transmitter and SKL3013 receiver

The modules use a 9-pin interface. SYS_WKP selects the FDR/HDR boot mode. An internal power-on delay reset circuit is provided.

RST uses 1.8 V logic and is active low.

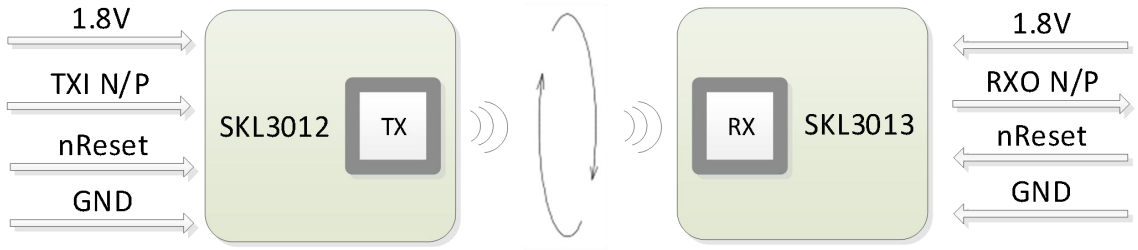

Figure 2. One-way wireless connection and coaxial rotation from SKL3012 to SKL3013

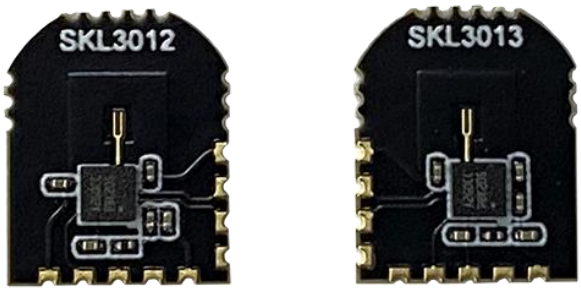

Figure 3. SKL3012 (left) and SKL3013 (right) photographs

5 Pin Definitions

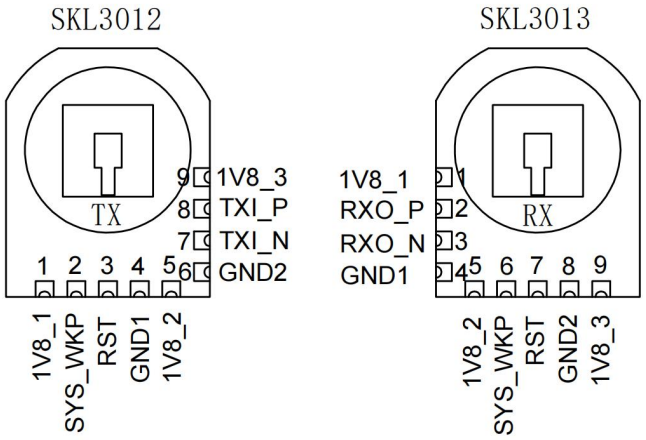

Figure 4. Nine-pin positions and signal labels for both models

Table 1. SKL3012 transmitter pin definitions

Pin No.	Signal Name	Description
1	1V8_1	1.8 V power input.
2	SYS_WKP	Boot configuration pin, 1.8 V logic; high selects FDR and low selects HDR.
3	RST	1.8 V active-low reset pin. Outputs the internal power-on delay reset signal, or accepts a low-level reset from host I/O. Leave unconnected when external reset is not required.
4	GND1	Ground.
5	1V8_2	1.8 V power input.

Pin No.	Signal Name	Description
6	GND2	Ground.
7	TXI_N	Transmit differential data input, negative.
8	TXI_P	Transmit differential data input, positive.
9	1V8_3	1.8 V power input.

Table 2. SKL3013 receiver pin definitions

Pin No.	Signal Name	Description
1	1V8_1	1.8 V power input.
2	RXO_P	Receive differential data output, positive.
3	RXO_N	Receive differential data output, negative.
4	GND1	Ground.
5	1V8_2	1.8 V power input.
6	SYS_WKP	Boot configuration pin, 1.8 V logic; high selects FDR and low selects HDR.
7	RST	1.8 V active-low reset pin. Outputs the internal power-on delay reset signal, or accepts a low-level reset from host I/O. Leave unconnected when external reset is not required.
8	GND2	Ground.
9	1V8_3	1.8 V power input.

Connect pins 1, 5 and 9 of both models to the 1.8 V supply. Connect the remaining ground and data pins according to Table 1、 Table 2. SKL3012 TXI_P/N are the transmit inputs from the host, and SKL3013 RXO_P/N are the module receive outputs.

6 Reference Design and Mode Configuration

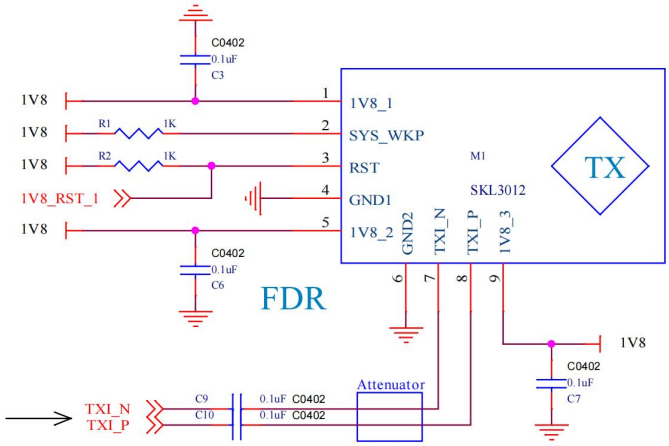

Figure 5. SKL3012 transmitter FDR reference circuit

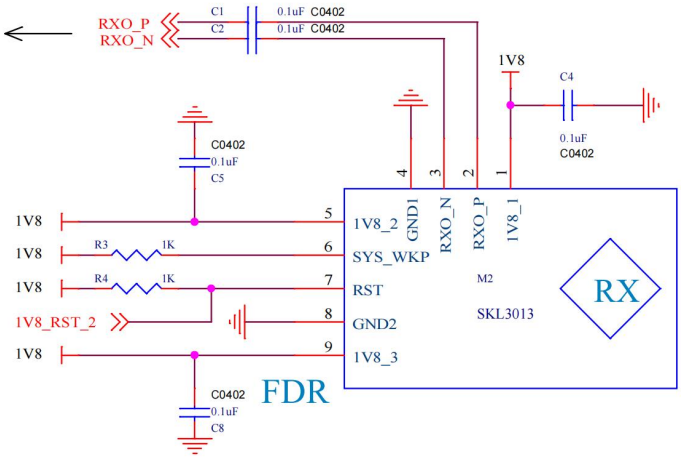

Figure 6. SKL3013 receiver FDR reference circuit

The example in Figure 5 and Figure 6 show connections with SYS_WKP pulled high to select FDR. Arrange supply decoupling and differential traces as illustrated. The RST pull-up shown is a reference connection; select the RST connection according to the reset-pin description in this datasheet. Place RXO output AC-coupling capacitors close to the module and TXI input AC-coupling capacitors close to the host as shown.

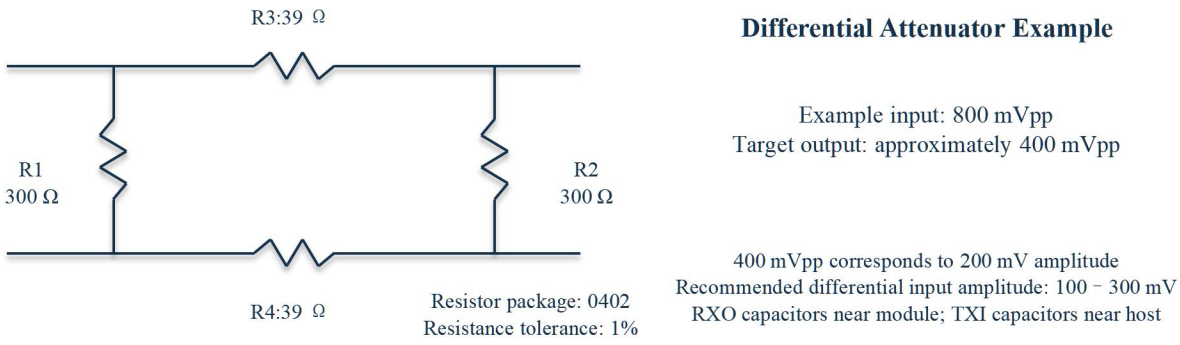

Figure 7. Differential input attenuation network and AC coupling

The example in Figure 7 illustrates 39 Ω series and 300 Ω shunt resistors with 1% tolerance, attenuating 800 mV differential peak-to-peak to approximately 400 mV peak-to-peak, equivalent to 200 mV differential amplitude.

Table 3. Hardware boot modes for standard products

SYS_WKP	Control Mode	Data Rate Mode	Interface rate range
1	HW-forced	FDR-DIFF	1 Mbit/s～5 Gbit/s
0	HW-forced	HDR-DIFF	500 Mbit/s～5.4 Gbit/s

(1) FDR-DIFF: SYS_WKP=1 selects forced hardware configuration; the interface rate is 1 Mbit/s–5 Gbit/s.

(2) HDR-DIFF: SYS_WKP=0 selects forced hardware configuration; the interface rate is 500 Mbit/s–5.4 Gbit/s.

Both FDR and HDR carry data through SLVS differential pairs. Select the same mode and compatible rates at both ends. SYS_WKP selects the boot mode at power-up.

Standard products use SYS_WKP hardware selection for FDR/HDR. I2C is used for internal configuration.

Use 8b/10b encoding for SLVS differential data at line rates above 100 Mbit/s. Before each new transmission, send an encoded, DC-balanced preamble in full before valid data. Its duration must allow link establishment and code-group synchronization. Refer to Reference Design Instructions in the companion user manual for encoding, idle and burst-timing details.

7 Electrical Characteristics

Table 4. Power supply and temperature parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IN}	Input voltage	1.7	1.8	1.98	V
I_{IN}	Input current (SKL3012/3013)	-	30	-	mA
T_A	Operating ambient temperature	−20	-	+85	°C

Table 5. Interface and RF parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IH}	Digital control input-high voltage	1.2	1.3	-	V
V_{IL}	Digital control input-low voltage	-	0.5	0.6	V
V_{DIFF_TX}	SLVS transmit-input differential voltage amplitude	100	200	300	mV
V_{CM_TX}	SLVS transmit-input common-mode voltage	160	-	310	mV
Z_{DIFF_TX}	SLVS transmit input differential impedance	-	100	-	Ω
V_{DIFF_RX}	SLVS receive-output differential voltage amplitude	80	200	300	mV
V_{CM_RX}	SLVS receive-output common-mode voltage	80	200	300	mV
Z_{DIFF_RX}	SLVS receive output differential impedance	-	100	-	Ω
F_{OSC}	Carrier frequency	-	60.6	-	GHz

The digital control pins use 1.8 V logic. The recommended SKL3012 transmit input differential amplitude is 100–300 mV and common-mode voltage is 160–310 mV. SKL3013 receive outputs use 100 Ω differential termination. Output amplitude is configurable from 80 to 300 mV, with 200 mV as the typical setting. Differential amplitude is the amplitude of the voltage difference between P and N; its peak-to-peak value is twice this amplitude.

The 1.7–1.98 V input voltage range is the recommended operating condition. The 30 mA input current is a typical value.

8 Assembly Instructions

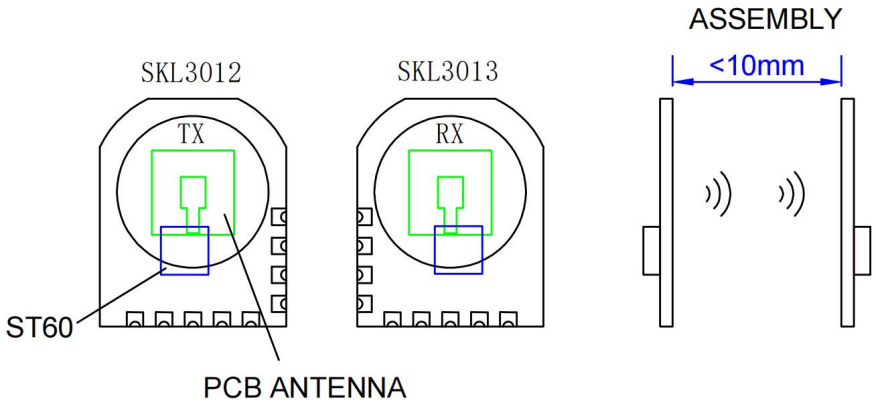

Figure 8. Paired assembly, antenna positions and spacing

Position the PCB patch antennas opposite each other and align them coaxially. The recommended spacing is approximately 5 mm. Follow Figure 8 to keep the assembly spacing below 10 mm. The rotary mechanism must maintain the relative antenna positions and an unobstructed signal path.

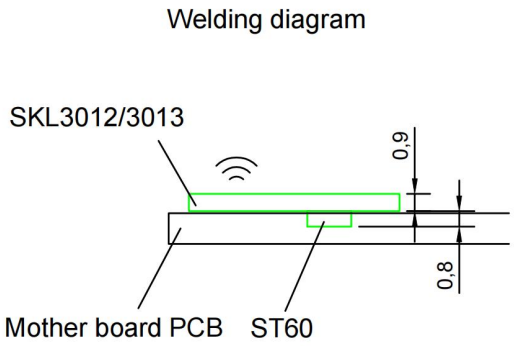

Figure 9. Module-to-host-PCB soldering cross-section (unit: mm)

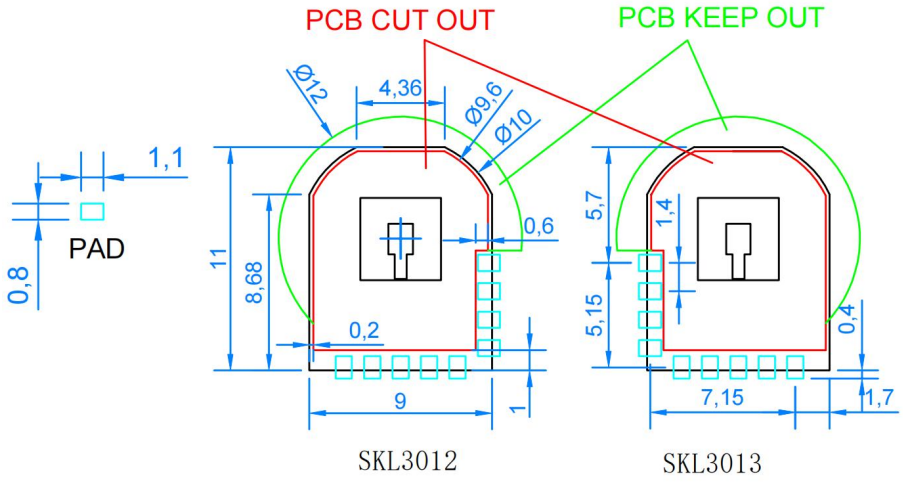

Figure 10. Host PCB cutout, pad and keep-out dimensions for both models (unit: mm)

The example in Figure 9 shows the module-to-host-PCB soldering cross-section. Follow Figure 10 to design the host PCB cutouts, nine pads and antenna keep-out areas for each model. PCB CUT OUT denotes the red cutout area, PCB KEEP OUT the green keep-out area, and PAD a solder pad.

When using a metal enclosure, provide a nonmetallic window in front of the millimeter-wave path. Keep the antenna faces opposite each other and coaxially aligned, with no metal obstructing the propagation path.

9 Product Model

Table 6. Product models

Product Models	Description
SKL3012	Simplex transmit castellated RF module with one integrated PCB patch antenna, differential data input, used in pairs.
SKL3013	Simplex receive castellated RF module with one integrated PCB patch antenna, differential data output, used in pairs.

10 Revision History

Date	Revision	Description of Changes
2019-08-05	V0.9	Initial draft.
2023-09-15	V1.0	Based on the SKA2P1 datasheet, with the SKA2P1 sections removed.
2023-10-31	V1.1	Updated assembly.
2026-11-04	V1.2	(1) Prepared the English datasheet from the reviewed Chinese edition; clarified one-way pairing between the SKL3012 transmitter and SKL3013 receiver and the maximum interface rate of 5.4 Gbit/s. (2) Described SYS_WKP selection of FDR/HDR and internal-only I2C configuration; organized complete pin tables, reference circuits and electrical parameters. (3) Briefly described the internal power-on delay reset and RST active level; standardized PCB patch antenna terminology and parameter symbols. (4) Organized photographs, pin diagrams and assembly drawings; standardized the Assembly Instructions section, figure numbering and references; translated historical revision descriptions for this English edition. (5) Equalized the Min., Typ. and Max. columns in parameter tables, retaining all values, conditions, units, font sizes and standard line spacing. (6) Arranged revision history entries from oldest to newest, preserving their original dates, revisions and descriptions. (7) Checked the destinations of contents entries and section, figure and table references; rebuilt Word/WPS-compatible internal bookmark links and corrected misplaced or invalid targets. (8) Refined the product overview to integrate the chipset platform naturally into the module, antenna and functional descriptions, retaining model-specific capabilities, pairing requirements and parameters. (9) Standardized chapter names, order and content allocation using the common outline, retaining technical descriptions and illustrations; updated the contents, figure/table numbering and internal references. (10) Prepared and checked this English edition against the current Chinese edition, preserving numbered items, parameters, illustrations, commands and operating instructions.