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SK-RF CO.,Ltd

DATASHEET

SKA2R1 Module Datasheet

60 GHz Half-Duplex Castellated RF Module

Document Type	Product Datasheet
Applicable Product	SKA2R1
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Document Summary: Describes the half-duplex link when SKA2R1 is paired with SKA2P1, pin definitions, boot modes, power supply and temperature conditions, reference circuits, and soldering and assembly dimensions for hardware selection and integration.

Contents

1 Product Overview
2 Features
3 Applications
4 Block Diagram and Appearance
5 Pin Definitions
6 Reference Design and Mode Configuration
7 Electrical Characteristics
8 Assembly Instructions
9 Product Model
10 Revision History

1 Product Overview

The SKA2R1 is a 60 GHz RF module built around the ST60A2 millimeter-wave transceiver, with an integrated circularly polarized PCB patch antenna. It mounts to the host PCB through castellated pads for centimeter-scale contactless data connections. When paired with an SKA2P1, it supports relative rotation with the antennas aligned on the same axis. An SKA2P1 can pair with another SKA2P1 or an SKA2R1; two SKA2R1 modules cannot communicate with each other. A single module pair operates in half duplex, with the host coordinating alternating transmission and reception at the two ends through RX_TX_MGT.

The module operates in half duplex. RX_TX_MGT uses 1.8 V logic: high selects transmit and low selects receive. The hosts coordinate alternating transmission and reception at both ends. Low-speed single-ended and high-speed SLVS differential data interfaces are provided.

2 Features

- 60 GHz V-band millimeter-wave communication with an integrated PCB patch antenna.
- HDR differential interface rate up to 6 Gbit/s; recommended antenna spacing approximately 10 mm.
- Half-duplex operation supporting coaxial rotary connection applications.
- Castellated pads for soldering to a host PCB.
- Hardware boot configuration and I2C control; GPIO-based direction control.
- Used in pairs with SKA2P1.

3 Applications

- Contactless high-speed connectors paired with SKA2P1
- Coaxial rotary connectors.

4 Block Diagram and Appearance

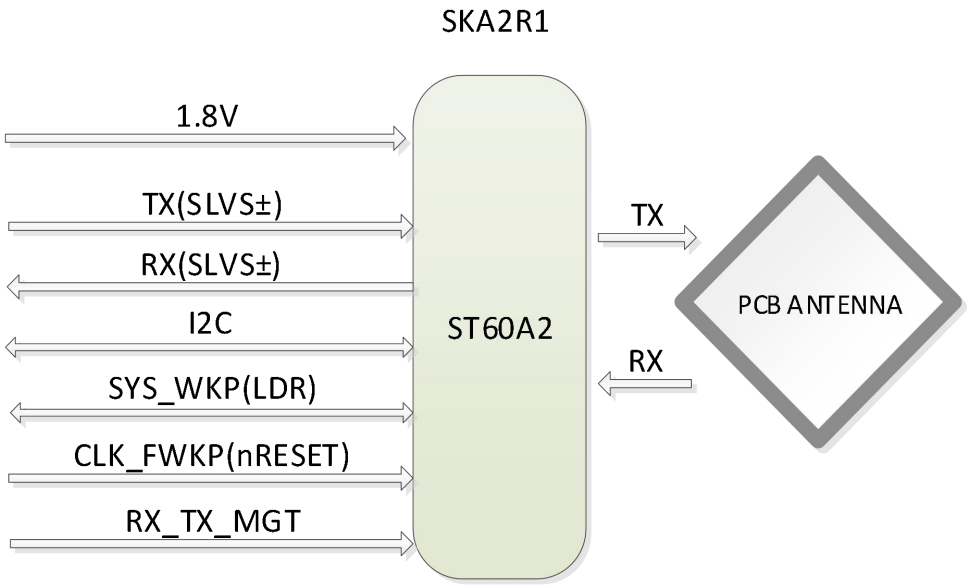


Figure 1. SKA2R1 internal functional block diagram

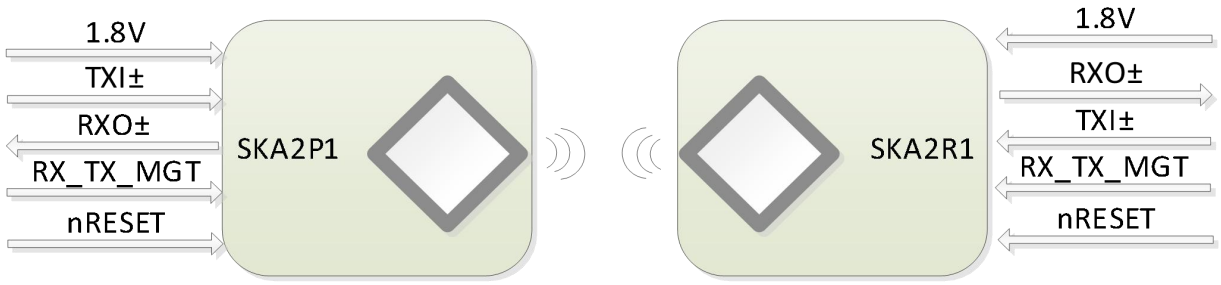


Figure 2. Paired connection of SKA2P1 and SKA2R1 (Half Duplex, Alternating Transmit/Receive)

TXI_P/TXI_N are the transmit differential inputs from the host to the module; RXO_P/RXO_N are the receive differential outputs from the module to the host. nRESET corresponds to CLK_FWKP; RX_TX_MGT selects the transmit/receive direction.

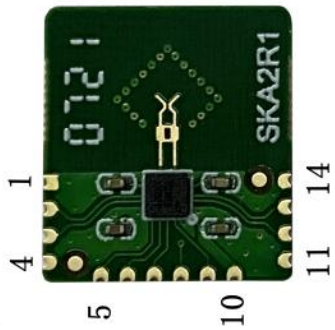


Figure 3. SKA2R1 module photograph

5 Pin Definitions

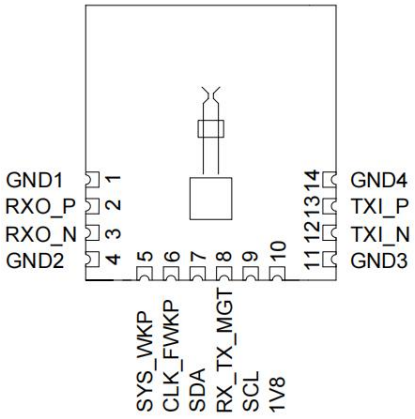


Figure 4. SKA2R1 pin layout

Table 1. Pin Definitions

Pin No.	Signal Name	Description
1	GND1	Ground.
2	RXO_P	Positive differential output for wirelessly received data.
3	RXO_N	Negative differential output for wirelessly received data.
4	GND2	Ground.

Pin No.	Signal Name	Description
5	SYS_WKP	LDR data input/output and boot-configuration pin; 1.8 V levels.
6	CLK_FWKP	Active-low reset. Keep low for at least 1 ms after the 1.8 V supply has stabilized.
7	SDA	I2C data and boot-configuration pin.
8	RX_TX_MGT	Direction control; 1.8 V levels. High: transmit; low: receive.
9	SCL	I2C clock and boot-configuration pin; 1.8 V levels.
10	1V8	1.8 V power input.
11	GND3	Ground.
12	TXI_N	Negative differential input to the wireless transmit channel.
13	TXI_P	Positive differential input to the wireless transmit channel.
14	GND4	Ground.

6 Reference Design and Mode Configuration

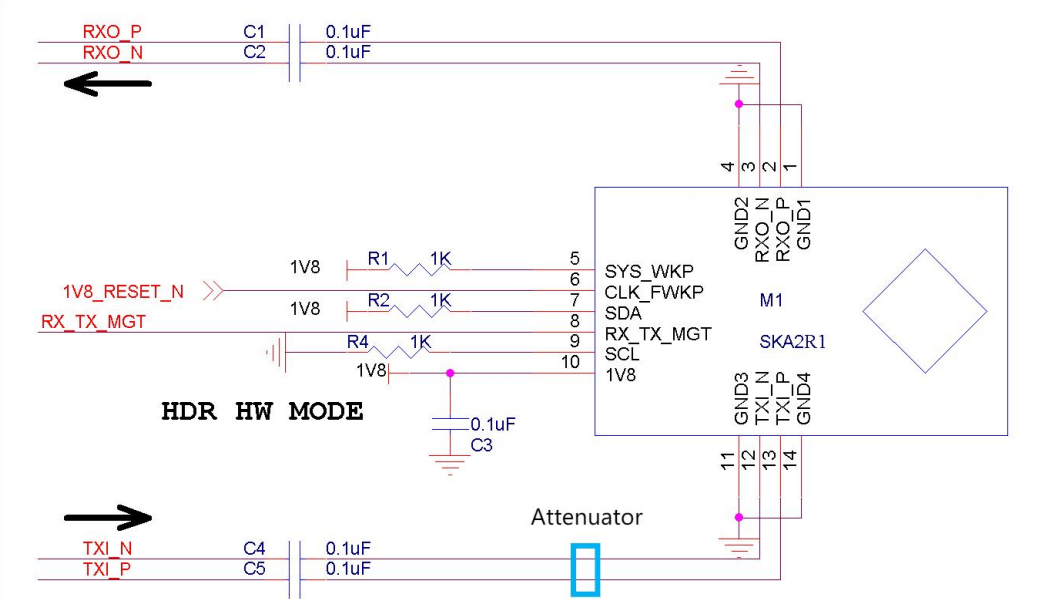


Figure 5. SKA2R1 HDR hardware mode reference circuit

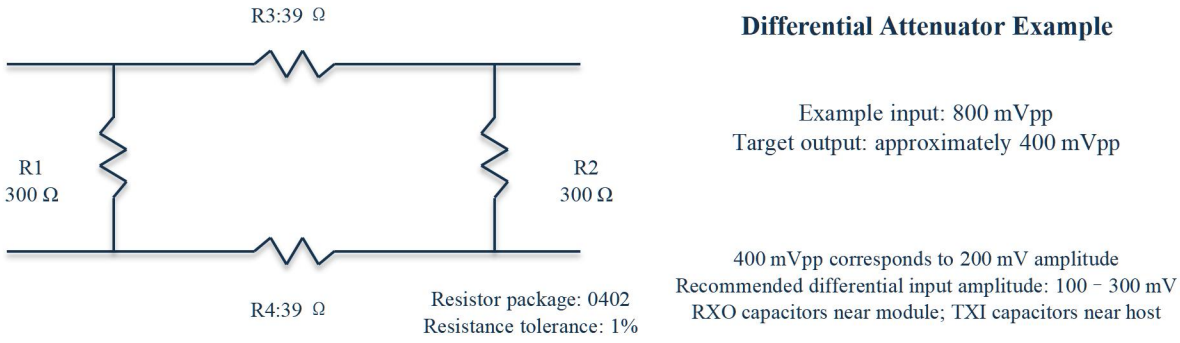


Figure 6. Input attenuation and AC-coupling reference

Place the RXO output AC-coupling capacitors close to the module and the TXI input capacitors close to the host. Figure 6 illustrates 39 Ω series and 300 Ω shunt resistors with 1% tolerance, attenuating 800 mV differential peak-to-peak to approximately 400 mV peak-to-peak, equivalent to 200 mV differential amplitude.

Table 2. Boot mode configuration

SCL	SDA	SYS_WKP	Control Mode	Data Rate Mode
0	0	Don't care	HW-forced	LDR-SE
0	1	1	HW-forced	FDR-DIFF
0	1	0	HW-forced	HDR-DIFF
1	Don't care	Don't care	I2C	Configurable via I2C

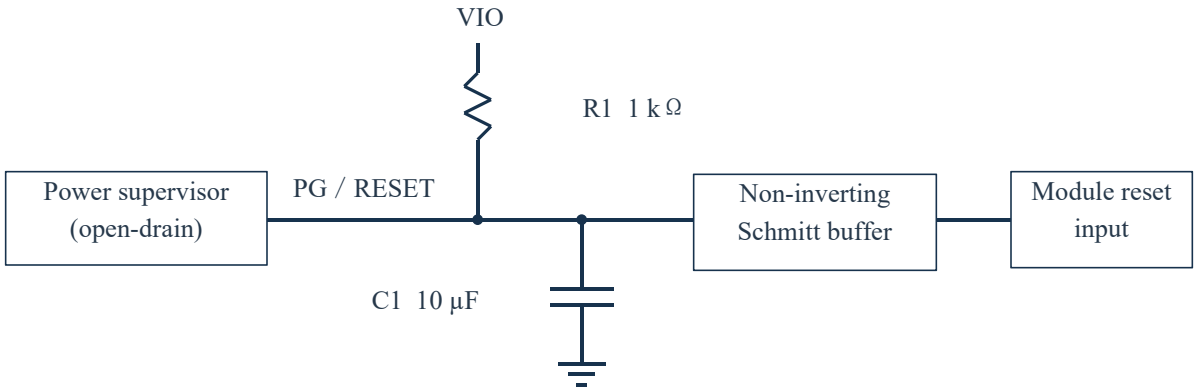
(1) LDR-SE: low-data-rate single-ended mode, 10 kbit/s–100 Mbit/s; data is carried on the SYS_WKP digital pin.

(2) FDR-DIFF: full-data-rate differential mode, 1 Mbit/s–5 Gbit/s; high-speed data is carried on SLVS differential pairs.

(3) HDR-DIFF: high-data-rate differential mode, 500 Mbit/s–6 Gbit/s; high-speed data is carried on SLVS differential pairs.

CLK_FWKP is an active-low reset. After the 1.8 V supply stabilizes, keep it low for at least 1 ms before releasing reset.

The host board may use the external RC reset circuit in Figure 7, with its output connected to CLK_FWKP. Recommended values are R1 = 1 kΩ and C1 = 10 µF, giving a nominal time constant of 10 ms. After the supply stabilizes, ensure that CLK_FWKP remains low for at least 1 ms and that the boot-strap levels are valid before releasing reset.



Select supervisor and buffer levels to suit the module interface. Connect all grounds together.

Figure 7. Recommended RC Reset Circuit

Use 8b/10b encoding for SLVS differential data at line rates above 100 Mbit/s. Before each new transmission, send an encoded, DC-balanced preamble in full before valid data. Its duration must allow link establishment and code-group synchronization. Refer to Reference Design Instructions in the companion user manual for encoding, idle and burst-timing details.

7 Electrical Characteristics

Table 3. Power supply and temperature parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IN}	Input voltage	1.7	1.8	1.98	V
I_{IN}	Input current*	-	30	-	mA
P	Total power consumption	-	0.054	-	W
T_A	Operating ambient temperature	−20	-	+85	°C
T_J	Maximum junction temperature	-	-	+125	°C
T_{STG}	Storage temperature	−40	-	+105	°C

Note*: The input current of 30 mA and total power consumption of 0.054 W are typical values with data transmission/reception at 5 Gbit/s.

Table 4. Digital Interface, SLVS and Carrier Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IH}	High-level input voltage	1.2	1.3	-	V
V_{OH}	High-level output voltage	1.6	-	-	V
V_{IL}	Low-level input voltage	-	0.5	0.6	V
V_{OL}	Low-level output voltage	-	-	0.2	V
V_{DIFF_TX}	SLVS transmit-input differential voltage amplitude	100	200	300	mV
V_{CM_TX}	SLVS transmit-input common-mode voltage	160	-	310	mV
Z_{DIFF_TX}	Transmit-input differential impedance	-	100	-	Ω
V_{DIFF_RX}	SLVS receive-output differential voltage amplitude	80	200	300	mV
V_{CM_RX}	SLVS receive-output common-mode voltage	80	200	300	mV
Z_{DIFF_RX}	Receive-output differential impedance	-	100	-	Ω
F_{OSC}	Carrier frequency	-	60.6	-	GHz

The digital control pins use 1.8 V logic. The output-high and output-low voltage specifications apply with a 5 mA load. The SLVS receive outputs use 100 Ω differential termination; the differential amplitude is configurable from 80 to 300 mV, with 200 mV listed as the typical setting. The transmit input common-mode voltage is 160–310 mV and the differential amplitude is 100–300 mV.

The SLVS differential voltage amplitude is the amplitude of the voltage difference between P and N; its peak-to-peak value is twice this amplitude. Receive output and transmit input refer to RXO and TXI, respectively. Follow Table 1.

8 Assembly Instructions

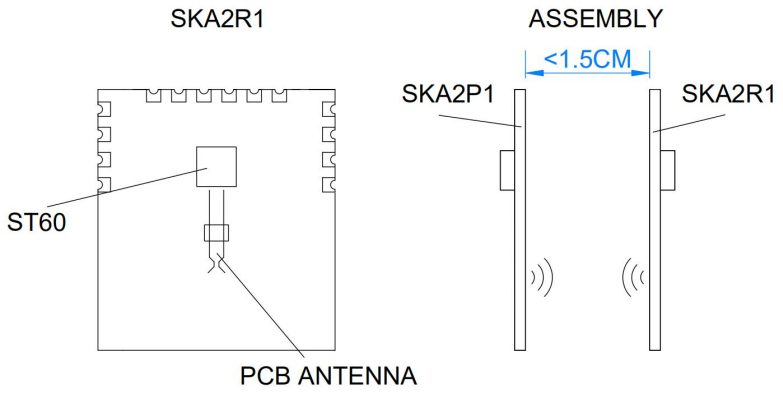


Figure 8. SKA2R1 antenna orientation and assembly spacing with SKA2P1

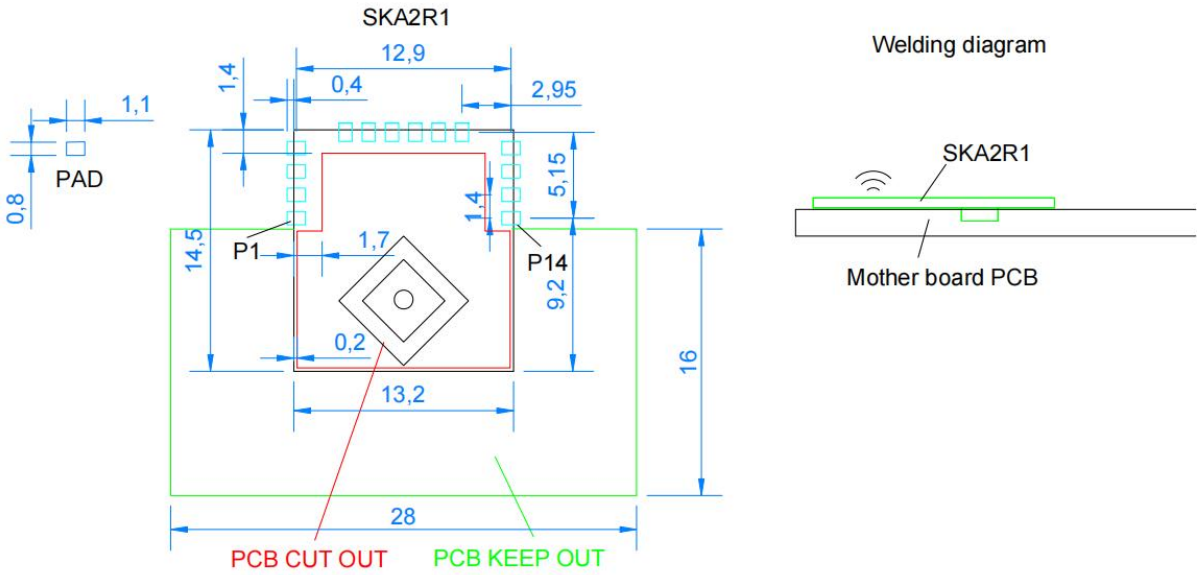


Figure 9. Host PCB cutout, keep-out and soldering dimensions (unit: mm)

Solder the module to the host PCB with the antenna side facing up and the chip side facing down. Follow Figure 9 to design the PCB CUT OUT and pads, retaining the P1–P14 pin orientation and dimensions. Mother board PCB denotes the host PCB; PCB KEEP OUT denotes the wireless keep-out area. The red area indicates the host PCB cutout.

The keep-out volume has a 16 mm × 28 mm base and a height equal to the spacing between the two antennas. Keep this volume free of metal parts, metallic paint, fasteners and other reflective obstructions.

Position the SKA2R1 and SKA2P1 antenna faces opposite each other and align them coaxially. Keep the assembly spacing below 15 mm; approximately 10 mm is recommended. Maintain axial spacing and coaxial alignment during rotation, and keep the millimeter-wave path free of metal obstructions.

9 Product Model

Table 5. Product Models

Product Models	Description
SKA2R1	Half-duplex castellated RF module with an integrated PCB patch antenna, used in pairs with SKA2P1.

10 Revision History

Date	Revision	Description of Changes
2019-08-05	V0.9	Initial draft.
2019-08-12	V1.0	Based on the SKA2x datasheet, with the SKA2Dxx sections removed.
2019-08-19	V1.1	Adjusted pad dimensions.
2019-08-21	V1.2	Corrected pad dimensions.
2020-08-19	V1.3	Removed two ground pads; updated the footprint and assembly method.
2021-04-13	V1.4	Updated the description of pin 8.
2021-04-20	V1.5	Updated the signal name for pin 8.
2021-06-11	V1.6	Based on the SKA2P1 datasheet, with the SKA2P1 sections removed.
2022-05-27	V1.7	Updated assembly.
2026-11-04	V1.9	(1) Prepared the English datasheet from the reviewed Chinese edition, clarifying the circularly polarized PCB patch antenna, pairing with SKA2P1 and coaxial relative rotation. (2) Organized half-duplex transmit/receive control, pin definitions, hardware modes and electrical parameters; standardized symbol subscripts, positive temperatures and missing-value notation. (3) Unified the minimum reset hold time to 1 ms; organized differential attenuation, AC-coupling and external RC reset reference circuits. (4) Added module photographs and pin diagrams; organized assembly, cutout and antenna spacing drawings; checked contents, figure numbering and references; translated historical descriptions for this English edition. (5) Standardized the bootstrap configuration table widths and layout using the SKA2Dxx user manual, retaining configuration values, pin aliases, font sizes, minimum row heights and cell margins. (6) Equalized the Min., Typ. and Max. columns in parameter tables, retaining all values, conditions, units, font sizes and standard line spacing. (7) Arranged revision history entries from oldest to newest, preserving their original dates, revisions and descriptions. (8) Checked the destinations of contents entries and section, figure and table references; rebuilt Word/WPS-compatible internal bookmark links and corrected misplaced or invalid targets. (9) Refined the product overview to integrate the chipset platform naturally into the module, antenna and functional descriptions, retaining model-specific capabilities, pairing requirements and parameters. (10) Standardized chapter names, order and content allocation using the common outline, retaining technical descriptions and illustrations; updated the contents, figure/table numbering and internal references. (11) Prepared and checked this English edition against the current Chinese edition, preserving numbered items, parameters, illustrations, commands and operating instructions.