V1.2 · 2026-11-04

SK-RF CO.,Ltd

USER MANUAL

SKA2P1 Module User Manual

Half-duplex module assembly, configuration and operation

Document Type	User assembly, configuration and operation manual
Applicable Product	SKA2P1
Release Date	2026-11-04
Document Version	V1.2

Document Summary: Instructions for SKA2P1 interface identification, soldering and assembly, power supply, boot configuration, transmit/receive direction control and connection checks, for hardware integration and host-side application development.

Contents

1 Functional Description

2 Pin Definitions

3 Electrical Characteristics

4 Reference Design

4.1 Peripheral Reference Circuit and Pin Connections

4.2 Reset Interface

4.3 TXI Attenuation and AC Coupling

4.4 8b/10b Data Encoding

4.5 Preamble and Burst-Data Timing

5 Mode Configuration

5.1 Boot Configuration

5.2 LDR-Mode Connection

5.3 FDR-Mode Connection

5.4 HDR-Mode Connection

6 Communication Connections

6.1 Simplex Communication

6.2 Half-Duplex Communication

6.3 Full-Duplex Communication

6.4 Communication Examples

7 Assembly Instructions

8 Power-Up and Operation

8.1 Initial Power-Up

9 Data Tests

10 Common Questions and Operating Checks

10.1 Common Questions and Corrective Actions

10.2 Technical Support

11 Revision History

1 Functional Description

SKA2P1 is a 60 GHz millimeter-wave castellated RF module with an integrated linearly polarized PCB patch antenna. It is soldered to a host board for centimeter-scale contactless data connections. SKA2P1 pairs with SKA2P1 or SKA2R1; two SKA2R1 modules cannot communicate with each other. A single pair operates in half duplex, with the host coordinating alternating transmit/receive operation through RX_TX_MGT.

Low-speed single-ended data is carried by SYS_WKP; high-speed data is carried by the SLVS differential interface. For Ethernet and similar applications, connect the appropriate PHY or SerDes on the host PCB and configure the interface rate and transmit/receive direction.

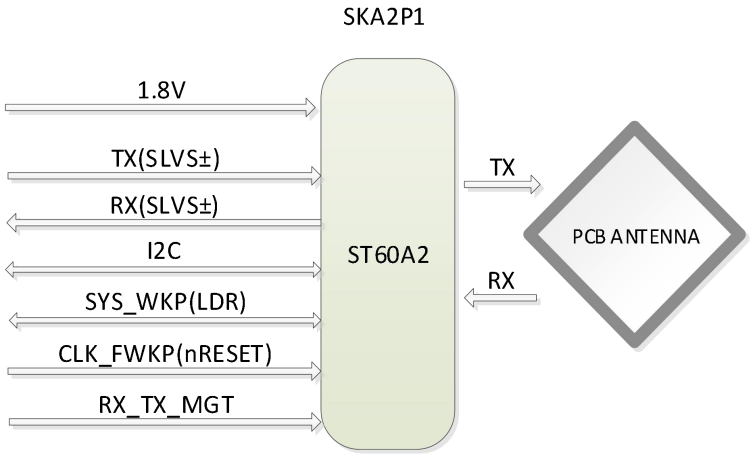


Figure 1. SKA2P1 Internal Block Diagram

2 Pin Definitions

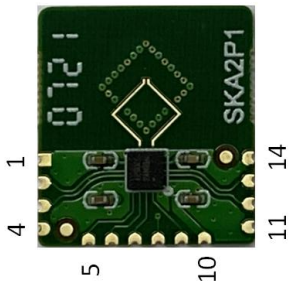


Figure 2. SKA2P1 photograph and pin orientation

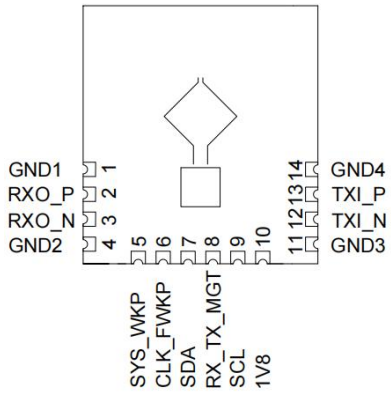


Figure 3. SKA2P1 pin layout (shared with SKA2R1)

Table 1. SKA2P1 pin definitions

Pin No.	Signal Name	Description
1	GND1	Ground.
2	RXO_P	Positive differential output for wirelessly received data.
3	RXO_N	Negative differential output for wirelessly received data.
4	GND2	Ground.
5	SYS_WKP	LDR data input/output and boot-configuration pin; 1.8 V levels.
6	CLK_FWKP	Active-low reset. Keep low for at least 1 ms after the 1.8 V supply has stabilized.
7	SDA	I2C data and boot-configuration pin.
8	RX_TX_MGT	Direction control; 1.8 V levels. High: transmit; low: receive.
9	SCL	I2C clock and boot-configuration pin; 1.8 V levels.
10	1V8	1.8 V power input.
11	GND3	Ground.
12	TXI_N	Negative differential input to the wireless transmit channel.
13	TXI_P	Positive differential input to the wireless transmit channel.
14	GND4	Ground.

3 Electrical Characteristics

Table 2. Power and Temperature Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IN}	Input voltage	1.7	1.8	1.98	V
I_{IN}	Input current*	-	30	-	mA
P	Total power consumption	-	0.054	-	W
T_A	Operating ambient temperature	−20	-	+85	°C
T_J	Maximum junction temperature	-	-	+125	°C
T_{STG}	Storage temperature	−40	-	+105	°C

Note*: The input current of 30 mA and total power consumption of 0.054 W are typical values with data transmission/reception at 5 Gbit/s.

Table 3. Digital Interface, SLVS and Carrier Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IH}	High-level input voltage	1.2	1.3	-	V
V_{OH}	High-level output voltage	1.6	-	-	V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	Low-level input voltage	-	0.5	0.6	V
V_{OL}	Low-level output voltage	-	-	0.2	V
V_{DIFF_TX}	SLVS transmit-input differential voltage amplitude	100	200	300	mV
V_{CM_TX}	SLVS transmit-input common-mode voltage	160	-	310	mV
Z_{DIFF_TX}	Transmit-input differential impedance	-	100	-	Ω
V_{DIFF_RX}	SLVS receive-output differential voltage amplitude	80	200	300	mV
V_{CM_RX}	SLVS receive-output common-mode voltage	80	200	300	mV
Z_{DIFF_RX}	Receive-output differential impedance	-	100	-	Ω
F_{OSC}	Carrier frequency	-	60.6	-	GHz

The digital control pins use 1.8 V logic; the digital output voltage specifications apply with a 5 mA load. The recommended SLVS transmit input differential amplitude is 100–300 mV and the common-mode voltage is 160–310 mV. The receive outputs use 100 Ω differential termination. Measure the voltage difference between P and N; its peak-to-peak value is twice its amplitude.

4 Reference Design

4.1 Peripheral Reference Circuit and Pin Connections

Wire by pin number: connect TXI_P/TXI_N to the local host transmit differential pair and RXO_P/RXO_N to the local host receive differential pair. Maintain the positive and negative polarity.

RX_TX_MGT uses 1.8 V logic: high selects transmit and low selects receive. SYS_WKP is used for LDR data input/output and boot configuration; SCL and SDA are used for I2C and the associated boot configuration.

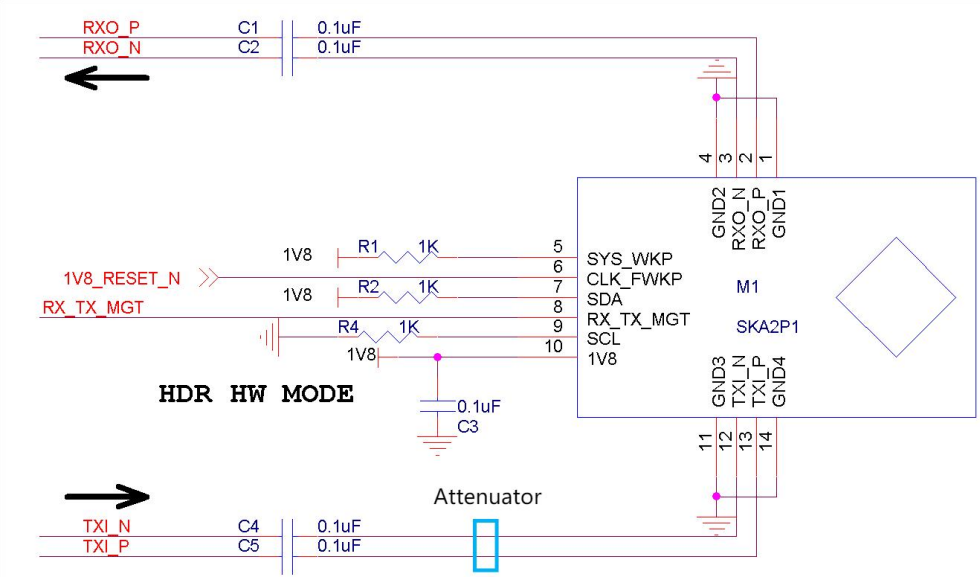
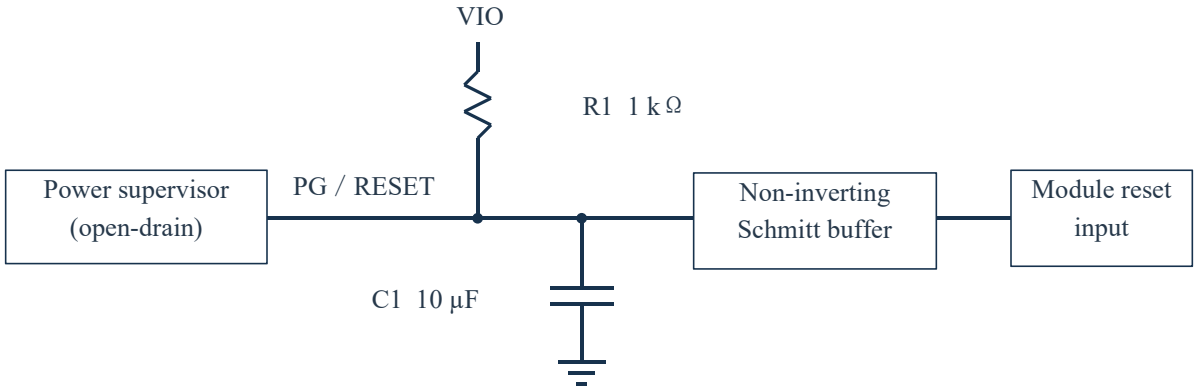


Figure 4. SKA2P1 peripheral reference circuit

4.2 Reset Interface

CLK_FWKP is an active-low reset. After the 1.8 V supply stabilizes, keep it low for at least 1 ms before releasing reset.

The host board may use the external RC reset circuit in Figure 5, with its output connected to CLK_FWKP. Recommended values are R1 = 1 kΩ and C1 = 10 µF, giving a nominal time constant of 10 ms. After the supply stabilizes, ensure that CLK_FWKP remains low for at least 1 ms and that the boot-strap levels are valid before releasing reset.



Select supervisor and buffer levels to suit the module interface. Connect all grounds together.

Figure 5. Recommended RC Reset Circuit

4.3 TXI Attenuation and AC Coupling

In SLVS differential mode, TXI accepts the host's differential signal. If the host output amplitude is excessive, an attenuator can bring the amplitude at the module input into the recommended range. LDR-SE uses the single-ended SYS_WKP data path and does not require this differential network.

Measure P−N differential peak-to-peak voltage at the module TXI input using the actual termination, operating rate and host output setting. The recommended input is 200–600 mVpp, equivalent to 100–300 mV differential amplitude. Within this range, use the reference connection directly. Above the upper limit, first reduce the host output setting; add attenuation if it remains excessive. Below the lower limit, check the host output setting and interconnect loss.

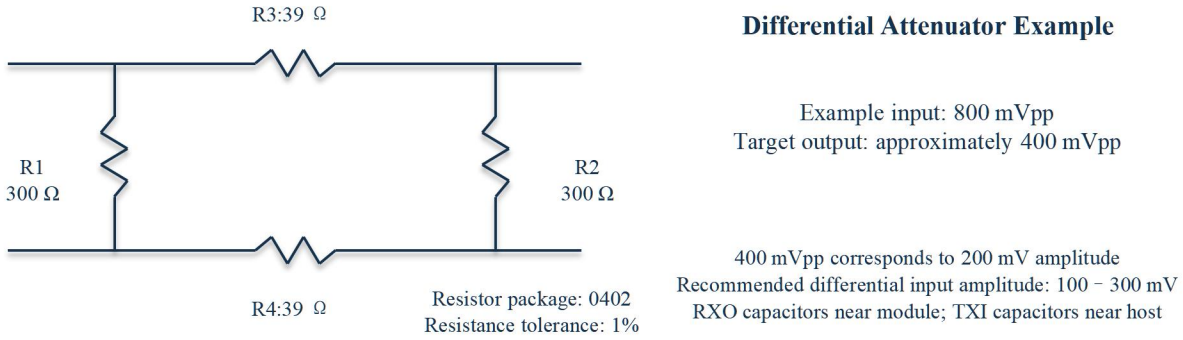


Figure 6. Differential input attenuation and AC-coupling reference

Use Figure 6. Insert 39 Ω in series with each P and N line, and connect 300 Ω across P/N at both ends of the network. Use 0402, 1% resistors and a symmetrical layout. Place TXI AC-coupling capacitors near the host, following this model's reference circuit.

The illustrated reduction from 800 mVpp to approximately 400 mVpp is a component-selection example. After assembly, remeasure differential peak-to-peak and common-mode voltages at TXI and verify data transfer. Check this model's electrical table and adjust resistance for the actual source impedance, termination and measurements.

4.4 8b/10b Data Encoding

Use 8b/10b encoding on the SLVS differential interface at line rates above 100 Mbit/s. Encoding is performed by the transmitting host, FPGA or SerDes, with corresponding decoding at the receiving host; the module carries the encoded serial signal. LDR single-ended data and differential data at or below 100 Mbit/s operate in their corresponding modes.

8b/10b maps each 8-bit data byte to a 10-bit line code group. The encoder selects valid codewords according to running disparity, maintaining DC balance and limiting consecutive identical bits to five. Sufficient transitions support receiver decisions and host clock recovery, avoiding errors caused by long runs of zeros, ones or biased data.

Use valid D code groups for data bytes and protocol-defined valid K code groups where control characters are required. The receiver checks code-group validity, running disparity and character boundaries before recovering payload data. During idle periods, send valid, DC-balanced encoded sequences and keep encoding rules consistent at both ends.

Line rate includes encoding overhead. For example, a 5 Gbit/s line provides at most 4 Gbit/s for 8b/10b data fields, before preamble, idle-character and protocol overhead. Record line rate and effective payload rate separately in host settings and test records.

64b/66b relies on scrambling for statistical DC balance and cannot directly replace the 8b/10b format required here. If the existing bus uses another encoding, adapt the format in the host or bridge logic before feeding the module's differential input.

4.5 Preamble and Burst-Data Timing

At the start of high-speed transmission, the receiver's adaptive decision threshold requires settling time. Send a continuous, DC-balanced, 8b/10b-encoded preamble before the payload, and start the application frame only after receiver decisions have stabilized. The preamble establishes the link and is not payload.

Preamble duration must cover receiver settling and code-group synchronization, with timing margin. Transmit the complete preamble before valid data begins.

Convert preamble duration to bits using the line rate: $N = \mathrm{ceil}(R \times t_{HEADER})$. R is in bit/s and t_{HEADER} is in seconds; round up to complete 10-bit code groups. At 5 Gbit/s, 50 ns and 90 ns correspond to 250 and 450 bits. At 500 Mbit/s, they correspond to 25 and 45 bits; send at least 30 and 50 bits respectively to complete the code groups.

Choose valid 8b/10b idle or training code groups allowed by the associated protocol, maintaining continuous running disparity. The illustrated alternating 0/1 sequence explains threshold settling; actual transmission must still use valid code groups and meet receive-character alignment requirements.

If transmission stops for longer than the selected t_{HEADER}, send the complete preamble again before the next transfer. In half-duplex operation, first switch the direction at both ends and allow device states to settle, then send the preamble and finally the payload. Meet direction-switching and preamble timing separately.

The receiving host accepts application data after the preamble ends and code-group/frame boundaries are confirmed. Test initial startup, restart after long idle, direction changes, different rates and the actual assembly gap. Record discarded training data, code-group errors, disparity errors and payload verification results separately.

5 Mode Configuration

5.1 Boot Configuration

SCL, SDA and SYS_WKP jointly determine the hardware boot mode. In Table 4, “Don’t care” means the mode does not depend on that pin's value. Provide stable boot-pin levels as required by the host PCB design.

(1) LDR-SE is the low-speed single-ended mode, carrying data through SYS_WKP at 1–100 Mbit/s.

(2) FDR-DIFF is the full-data-rate differential mode, covering 1 Mbit/s–5 Gbit/s;

(3) HDR-DIFF is the high-data-rate differential mode, covering 500 Mbit/s–6 Gbit/s. Both high-speed modes use SLVS differential inputs and outputs.

Table 4. Boot mode configuration

SCL	SDA	SYS_WKP	Control Mode	Data Rate Mode
0	0	Don't care	HW-forced	LDR-SE
0	1	1	HW-forced	FDR-DIFF
0	1	0	HW-forced	HDR-DIFF
1	Don't care	Don't care	I2C	Configurable via I2C

In LDR mode, GPIO data is carried through SYS_WKP and RX_TX_MGT controls the transmit/receive direction. See Figure 15. Figure 16 uses two pairs of modules and external PHYs to carry 1 Gbit/s Ethernet interface data in each direction.

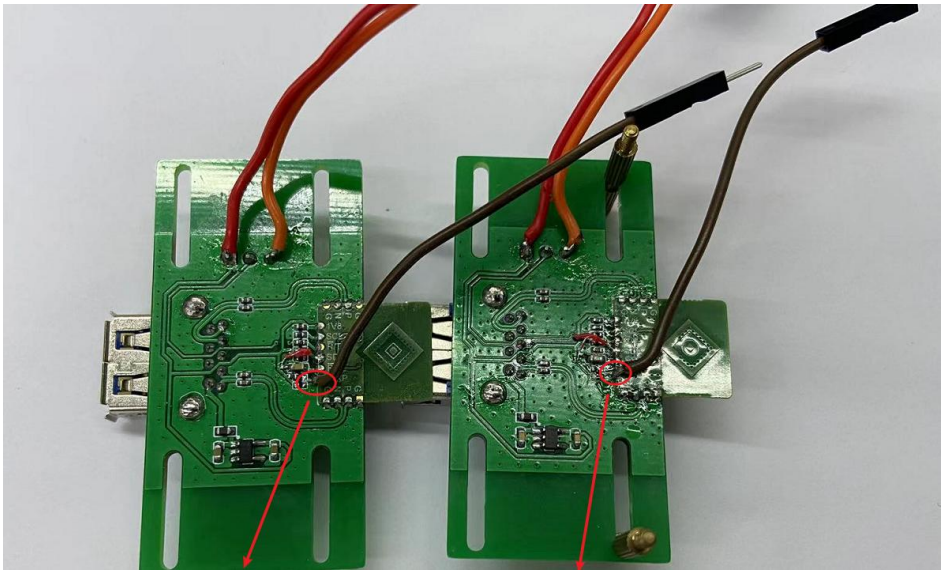


Figure 7. SYS_WKP measurement points (left: RX; right: TX)

During bootstrap configuration, SYS_WKP is an input. In LDR mode, it is a data input in transmit mode and a data output in receive mode. It carries data and is not a dedicated link-status indicator.

In the transmit-mode LDR test, SYS_WKP was observed to remain high with no external data source connected to the pin. When connected to a UART host, the pin is driven by the host and carries transmit data. The host must provide valid levels compatible with 1.8 V logic; leaving the pin unconnected is not a substitute for driving the data input.

In the SKA2P1 UART test with a high idle level, the receive-side SYS_WKP measured approximately 0 V before the first data was received. After the first data transfer, it measured approximately 1.8 V while idle and toggled with

received data. These observations apply to the stated test conditions. Verify communication using known data, the received waveform and data integrity checks, rather than the static SYS_WKP level alone.

5.2 LDR-Mode Connection

Set SCL = 0 and SDA = 0. SYS_WKP serves as a 1.8 V single-ended data pin. Connect the two ends according to their channel directions and use this model's control interface when switching direction.

LDR boot: SCL = 0; SDA = 0; SYS_WKP carries data



Single-pair half-duplex; coordinate RX_TX_MGT at both ends to alternate transmission and reception

Figure 8. SKA2P1 LDR mode communication and boot connections

5.3 FDR-Mode Connection

Set SCL = 0, SDA = 1 and SYS_WKP = 1. Payload data is carried on TXI/RXO differential interfaces.

FDR boot: SCL = 0; SDA = 1; SYS_WKP = 1



Single-pair half-duplex; coordinate RX_TX_MGT at both ends to alternate transmission and reception

Figure 9. SKA2P1 FDR mode communication and boot connections

5.4 HDR-Mode Connection

Set SCL = 0, SDA = 1 and SYS_WKP = 0. Payload data is carried on TXI/RXO differential interfaces.

HDR boot: SCL = 0; SDA = 1; SYS_WKP = 0



Single-pair half-duplex; coordinate RX_TX_MGT at both ends to alternate transmission and reception

Figure 10. SKA2P1 HDR mode communication and boot connections

6 Communication Connections

6.1 Simplex Communication

For one-way transmission, use one module as the transmitter and the other as the receiver. Set RX_TX_MGT high at the transmitting end and low at the receiving end. In differential mode, connect the data source to the transmitter TXI differential pair and the receiver RXO differential pair to the data-receiving device. The two one-way connection arrangements are shown in Figure 11、 Figure 12.

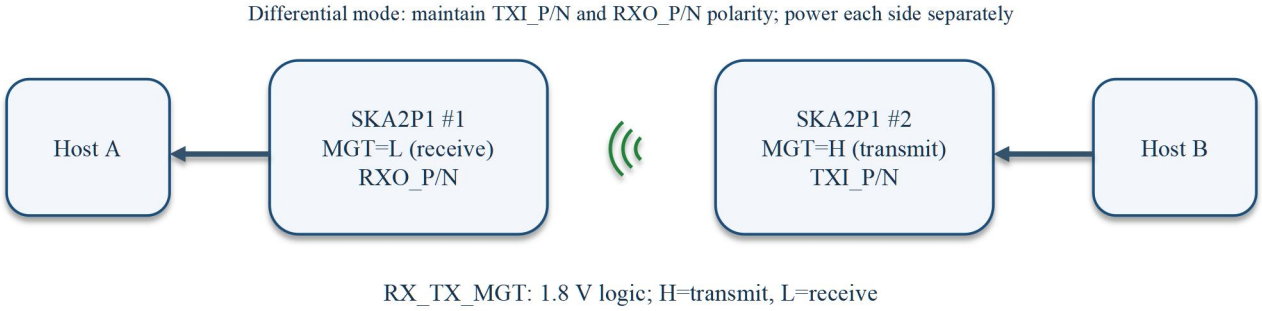


Figure 11. One-way connection: end B transmits and end A receives

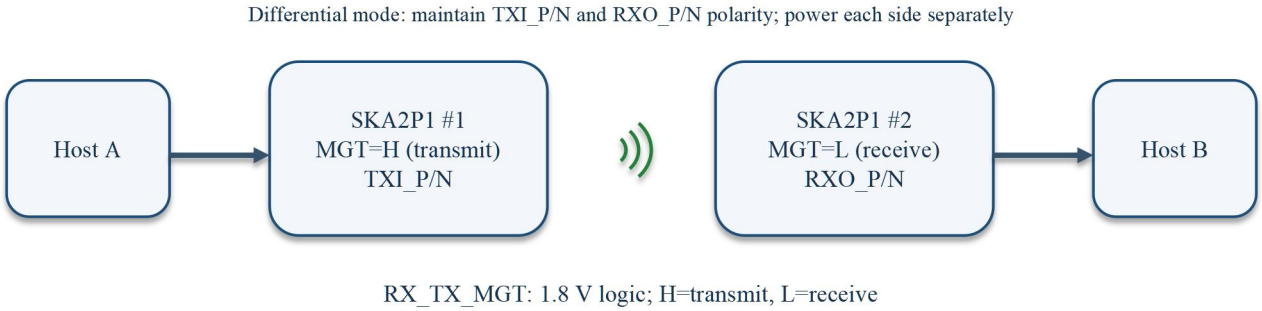


Figure 12. One-way connection: end A transmits and end B receives

6.2 Half-Duplex Communication

Connect TXI and RXO of one module pair to the hosts on the two sides to form a time-division bidirectional channel. Before transmitting, the host sets the local RX_TX_MGT high and the opposite end low. Coordinate switching at both ends when reversing direction so that the transmitting and receiving ends match.

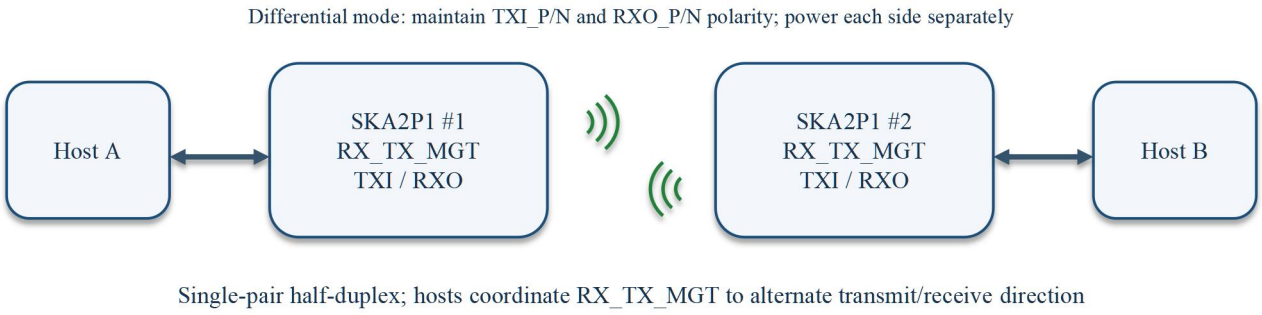


Figure 13. Half-duplex connection using one module pair

6.3 Full-Duplex Communication

For full-duplex operation, use two pairs of modules to form one-way channels in opposite directions. One pair carries A→B and the other carries B→A. Set each channel's transmitting module high and receiving module low. The four-module arrangement is shown in Figure 14.

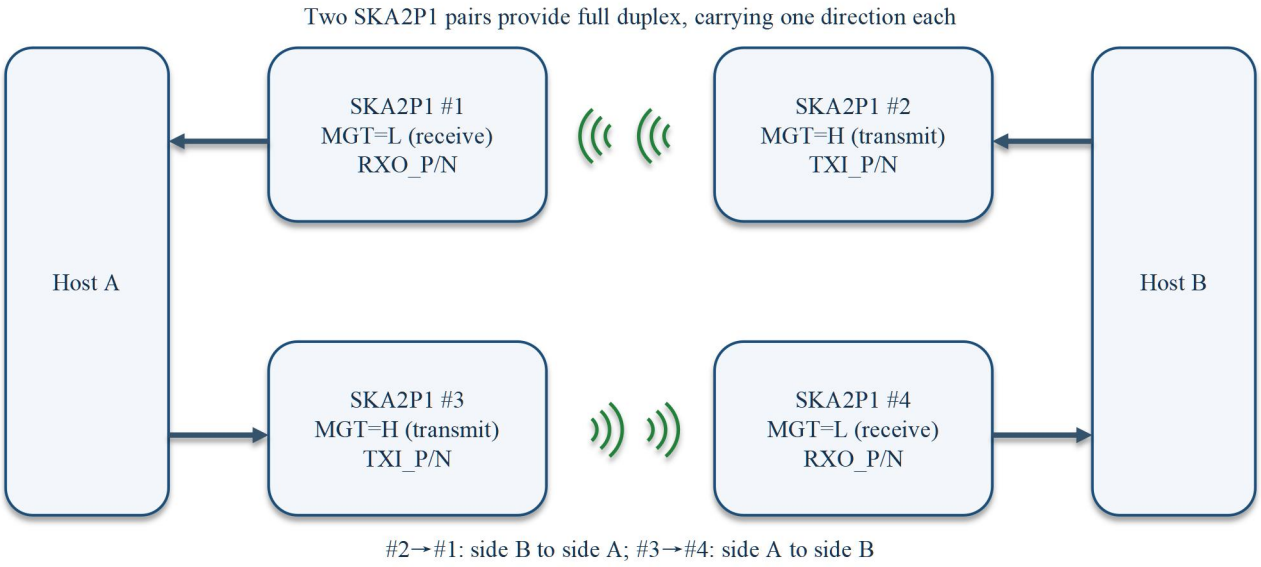


Figure 14. Two module pairs forming one-way channels in opposite directions

6.4 Communication Examples

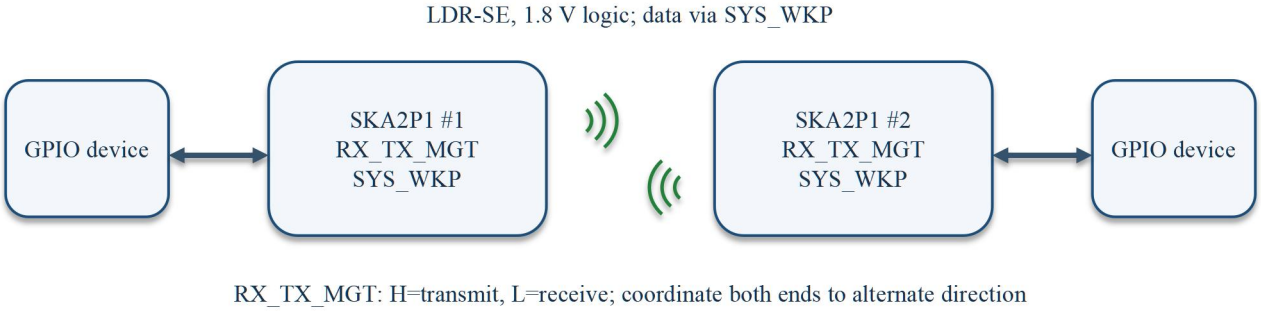


Figure 15. LDR mode GPIO communication and transmit/receive direction

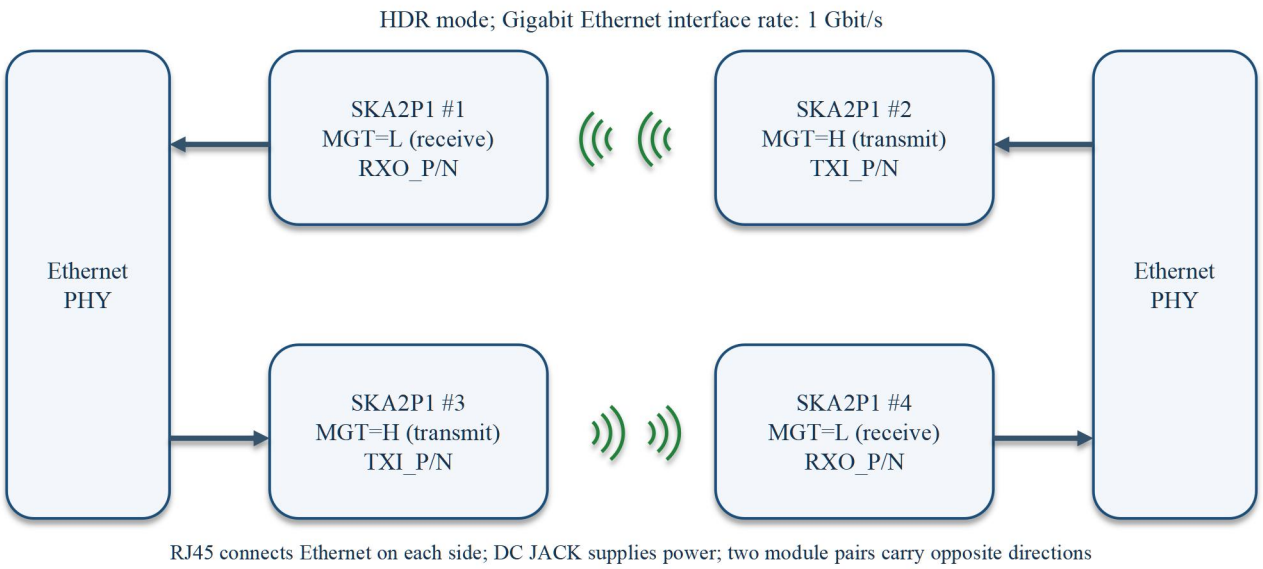


Figure 16. Example HDR mode contactless Gigabit Ethernet system

7 Assembly Instructions

Solder the module to the host PCB with the antenna side facing up and the chip side facing down. Design the PCB CUT OUT using the original host PCB cutout and pad drawing, retaining the P1–P14 orientation, pad dimensions and cutout boundaries.

PCB KEEP OUT denotes the wireless keep-out volume, with a 16 mm × 28 mm base and a height equal to the antenna spacing. Remove metal parts, screws, metallic paint and other reflective objects from this volume. Secure cables and electronic components to keep them out of the propagation path.

Position the antenna faces opposite each other and align their centers. Keep the assembly spacing below 15 mm; approximately 10 mm is recommended. For cutout dimensions and soldering orientation, see Figure 17; for antenna orientation and spacing, see Figure 18.

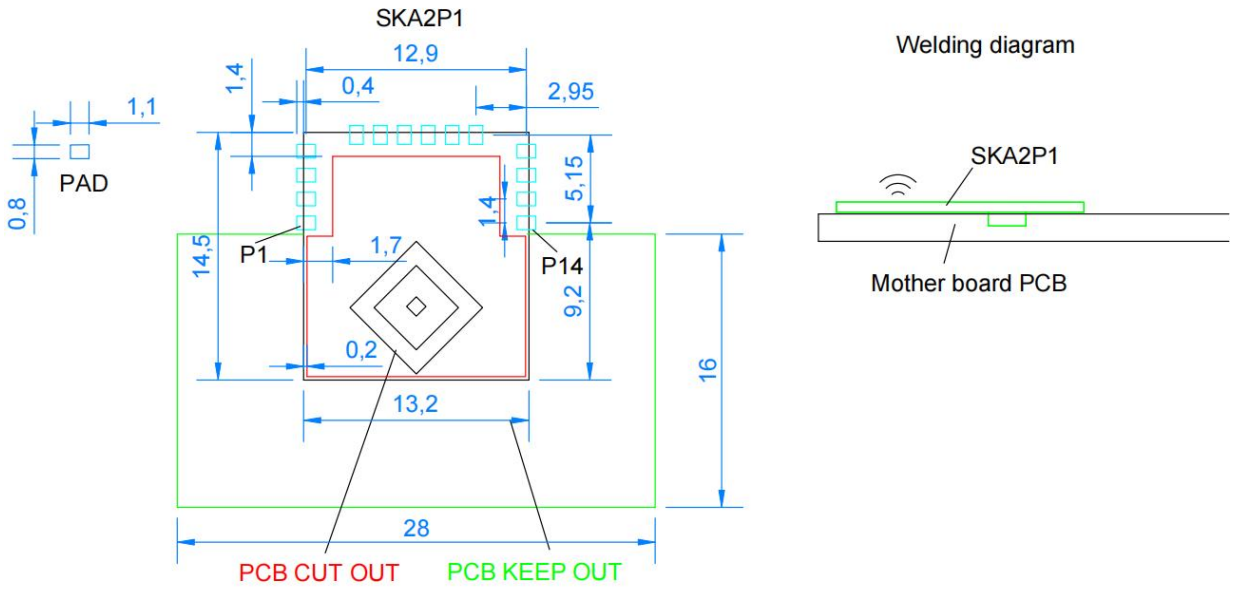


Figure 17. Host PCB cutout, antenna keep-out and soldering dimensions (unit: mm)

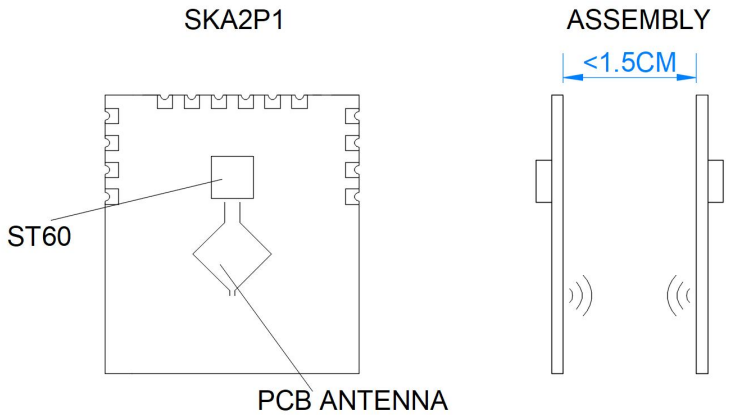


Figure 18. Antenna orientation and assembly spacing (unit: mm)

8 Power-Up and Operation

8.1 Initial Power-Up

(1) With power disconnected, check the pins, solder joints, cutout, antenna orientation and assembly spacing. Ensure that the keep-out area is free of metal obstructions.

(2) Check that the supply is within the recommended 1.7–1.98 V range, with a typical value of 1.8 V. Check polarity, grounding and external data interface levels.

(3) Select the data mode and connection arrangement for the application, configure the boot pins and coordinate the transmit/receive directions at both ends. In differential mode, check TXI/RXO polarity; in LDR mode, check the SYS_WKP data path.

(4) After power-up, wait for the 1.8 V supply to stabilize and keep CLK_FWKP low for at least another 1 ms, then release reset. Perform the required host-system configuration.

(5) Check the transmitting and receiving ends using known data. For bidirectional applications, verify forward and reverse transmission and direction switching separately. Save the configuration and data statistics.

Before power-up, check differential input levels as described in Section 4.3. Reset connections and timing are described in Section 4.2.

9 Data Tests

First secure both antennas at approximately 10 mm spacing, and configure the same data mode and compatible rates.

(1) One-way connection: use a fixed data pattern or application data; record transmitted and received quantities and error statistics. Reverse the transmit/receive direction and repeat.

(2) Half-duplex bidirectional connection: alternate host transmission and reception, continuously checking data after each direction switch. Record control states, data lengths and losses.

(3) Full duplex with two module pairs: verify each one-way channel separately before transmitting in both directions simultaneously. Save separate statistics for each direction.

(4) Repeat testing at the target spacing, with the actual enclosure and operating temperature. Record the mode, interface rate, spacing, offset, window material, temperature and duration.

(5) After maintenance or structural changes, recheck the supply, reset and boot-pin levels before repeating the same data tests.

For bit-error testing, record the transmitted and erroneous bit counts. For packet-based applications, record packet counts, packet loss and checksum errors separately. Retain both host configurations, raw statistics and assembly photographs together.

10 Common Questions and Operating Checks

10.1 Common Questions and Corrective Actions

Table 5. Troubleshooting

Symptom	Checks and Corrective Action
No data	Check supply and ground, a reset-low hold time of at least 1 ms, boot mode, RX_TX_MGT direction at both ends and TXI/RXO wiring. Check P/N polarity in differential mode and SYS_WKP in LDR mode.
Only one direction works	Check transmit/receive control and coordinated switching in each direction. For full duplex using two module pairs, verify the two one-way channels separately before simultaneous bidirectional transmission.
Increased high-speed data errors	Check differential input amplitude, common-mode voltage, 100 Ω termination, AC-coupling capacitors and the attenuation network.
Unstable link	Check face-to-face antenna placement, spacing, alignment, mechanical fixing and antenna keep-out. Repeat the tests in the Data Testing section and retain fault records.

10.2 Technical Support

When contacting technical support, provide the product model and revision, connections and settings at both ends, power-supply conditions, indicator states, symptoms and steps to reproduce the issue. Include wiring and assembly photographs, test settings and recorded results.

11 Revision History

Date	Revision	Description of Changes
2021-04-20	V0.9	Initial draft.
2023-06-02	V1.0	Corrected block diagram naming.
2024-12-17	V1.1	Updated LDR mode applications.
2026-11-04	V1.2	(1) Organized the English user manual from the reviewed Chinese edition with complete pin definitions, electrical characteristics, reference design, mode configuration, communication, assembly, power-up and data testing instructions. (2) Clarified P1/P1 and P1/R1 pairing, half-duplex direction control and LDR mode SYS_WKP levels; retained photographs, pin diagrams and assembly drawings. (3) Added separate subsections for TXI attenuation and AC coupling, the minimum 1 ms reset hold time and the external 1 kΩ/10 µF RC reset; added 8b/10b encoding and preamble timing. (4) Organized LDR/FDR/HDR mode diagrams and simplex, half-duplex and two-pair full-duplex connection diagrams; separated the GPIO and Ethernet communication examples. (5) Expanded data testing and troubleshooting, checked contents and figure/table references, and standardized device frames, arrows and wireless symbols in editable connection diagrams. (6) Standardized the bootstrap configuration table widths and layout using the SKA2Dxx user manual, retaining configuration values, pin aliases, font sizes, minimum row heights and cell margins. (7) Equalized the Min., Typ. and Max. columns in parameter tables, retaining all values, conditions, units, font sizes and standard line spacing. (8) Arranged revision history entries from oldest to newest, preserving their original dates, revisions and descriptions. (9) Checked the destinations of contents entries and section, figure and table references; rebuilt Word/WPS-compatible internal bookmark links and corrected misplaced or invalid targets. (10) Standardized chapter names, order and content allocation using the common outline, retaining technical descriptions and illustrations; updated the contents, figure/table numbering and internal references. Moved initial power-up under Power-Up and Operation, standardized Common Questions and Operating Checks, and added the information required for technical support. (11) Prepared and checked this English edition against the current Chinese edition, preserving numbered items, parameters, illustrations, commands and operating instructions. (12) Updated the LDR SYS_WKP description to include the observed high level with the transmit input unconnected; clarified host-driven data input, receive-side test conditions and communication checks, and corrected the measurement-point illustration.