V1.5 · 2026-11-03

SK-RF CO.,Ltd

DATASHEET

SKA2Dxx Module Datasheet

60 GHz Full-Duplex Castellated RF Modules

Document Type	Product Datasheet
Applicable Product	SKA2DHV / SKA2DVH
Release Date	2026-11-03
Document Version	V1.5

Document Summary: Product functions, data interfaces, boot configuration, electrical characteristics, reference circuits and mounting dimensions of SKA2DHV/SKA2DVH for hardware design and system integration.

Contents

1 Product Overview
2 Features
3 Applications
4 Block Diagram and Appearance
5 Pin Definitions
6 Reference Design and Mode Configuration
7 Electrical Characteristics
8 Assembly Instructions
9 Product Model
10 Revision History

1 Product Overview

The SKA2Dxx family comprises 60 GHz RF modules built around the ST60A2 millimeter-wave transceiver, with horn antennas of complementary polarizations. The modules mount to the host PCB through castellated pads. An SKA2DHV and an SKA2DVH operate as a pair, converting host data to millimeter-wave signals to establish a bidirectional full-duplex contactless link across a centimeter-scale gap.

The modules provide low-speed single-ended and high-speed SLVS differential data interfaces, with hardware boot configuration and I2C control. Interface rates for LDR, FDR and HDR modes are listed in Table 2.

2 Features

- 60 GHz V-band millimeter-wave communication.
- Bidirectional full-duplex operation with paired modules.
- Castellated pads for soldering onto a host board.
- I2C and GPIO-related boot configuration; 1.8 V control logic.
- Up to 6 Gbit/s in HDR differential mode and 5 Gbit/s in FDR differential mode.
- Recommended transmission gap: approximately 2 cm; mounting gap must be less than 30 mm.

3 Applications

- Contactless high-speed connectors.

4 Block Diagram and Appearance

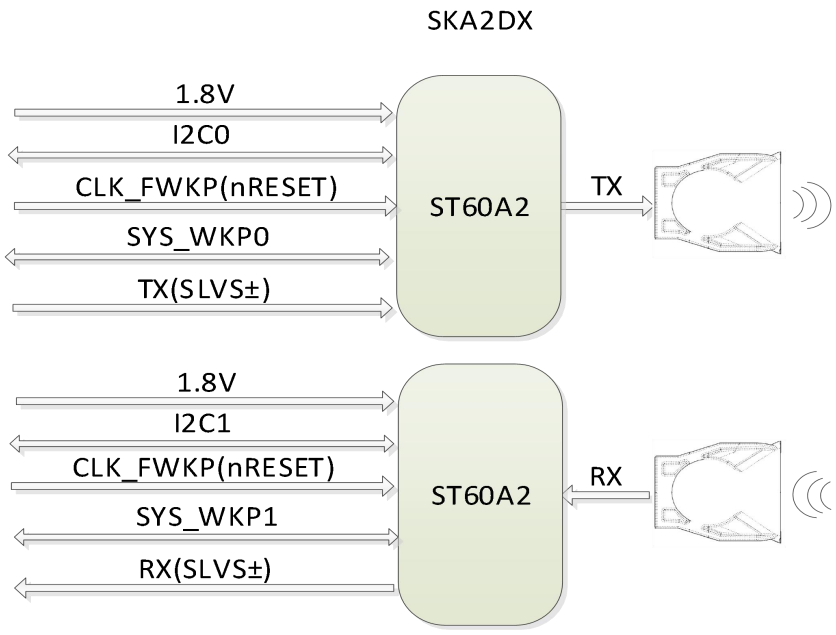


Figure 1. SKA2Dxx Internal Block Diagram

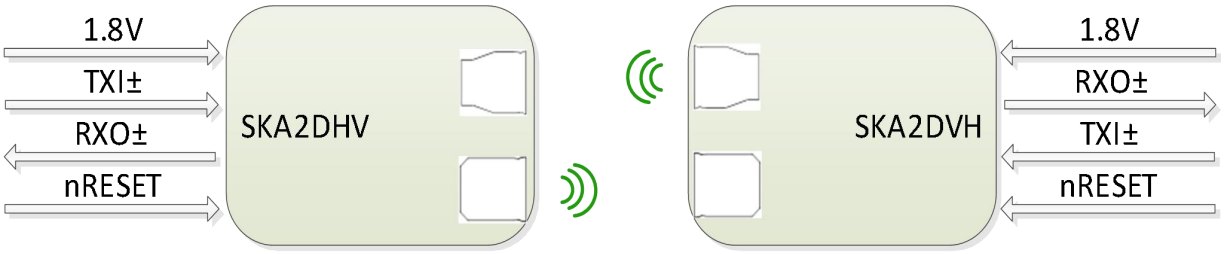


Figure 2. Paired SKA2DHV/SKA2DVH Connection

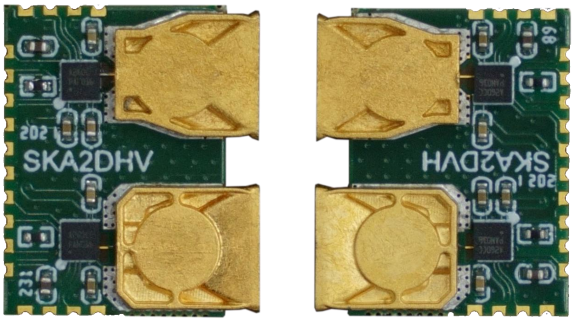


Figure 3. SKA2Dxx Module Photograph

TXI_P/TXI_N are differential inputs carrying data into the module for wireless transmission; RXO_P/RXO_N are differential outputs carrying wirelessly received data. Use complementary antenna polarizations and align the two modules correctly.

5 Pin Definitions

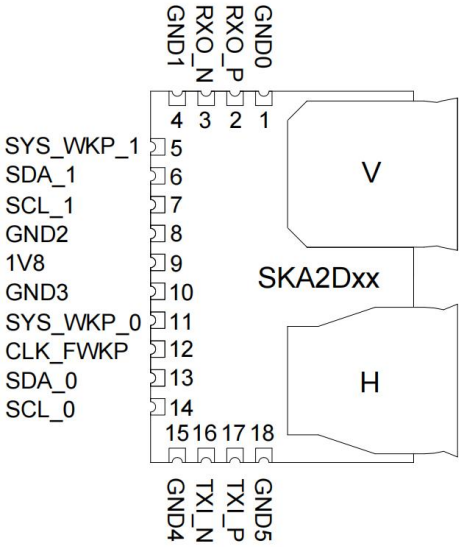


Figure 4. SKA2Dxx Pin Layout

Table 1. Pin Definitions

Pin No.	Signal Name	Description
1	GND0	Ground.
2	RXO_P	Positive differential output for wirelessly received data.

Pin No.	Signal Name	Description
3	RXO_N	Negative differential output for wirelessly received data.
4	GND1	Ground.
5	SYS_WKP_1	Boot configuration pin; 1.8 V logic.
6	SDA_1	Boot configuration pin; 1.8 V logic.
7	SCL_1	Boot configuration pin; 1.8 V logic.
8	GND2	Ground.
9	1V8	1.8 V power input.
10	GND3	Ground.
11	SYS_WKP_0	Boot configuration pin; 1.8 V logic.
12	CLK_FWKP	Active-low reset. Keep low for at least 1 ms after the 1.8 V supply has stabilized.
13	SDA_0	Boot configuration pin; 1.8 V logic.
14	SCL_0	Boot configuration pin; 1.8 V logic.
15	GND4	Ground.
16	TXI_N	Negative differential input to the wireless transmit channel.
17	TXI_P	Positive differential input to the wireless transmit channel.
18	GND5	Ground.

6 Reference Design and Mode Configuration

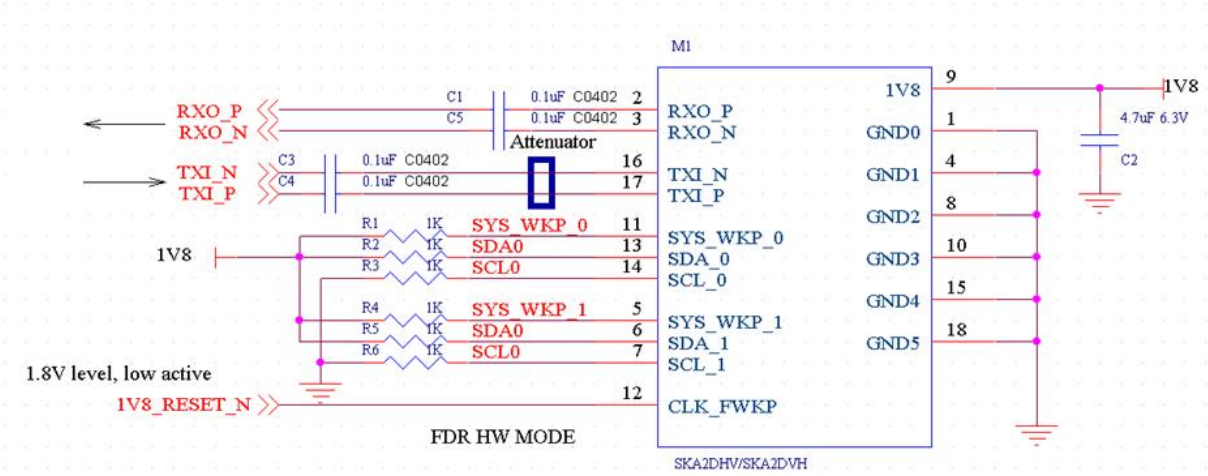


Figure 5. Module Reference Connections

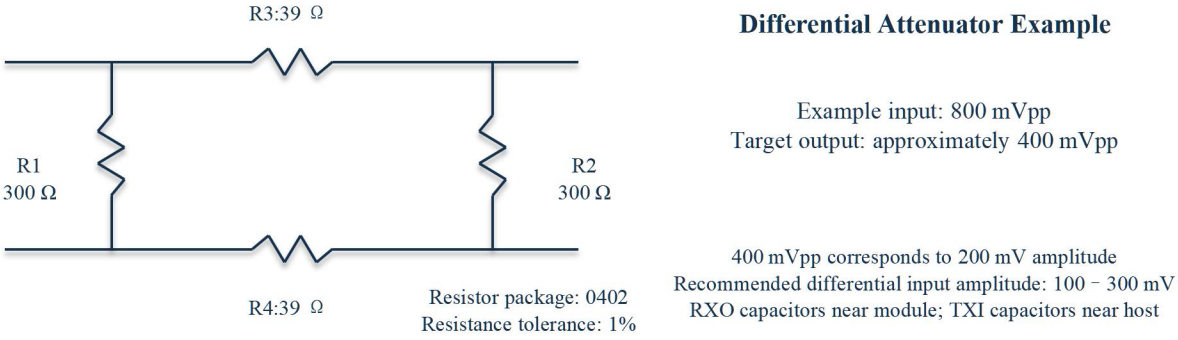


Figure 6. Differential Attenuation and AC-Coupling Reference

Place the RXO output AC-coupling capacitors near the module and the TXI input AC-coupling capacitors near the host. Figure 6 uses 39 Ω series and 300 Ω shunt resistors in 0402 packages to attenuate 800 mV differential peak-to-peak to approximately 400 mV peak-to-peak, equivalent to a differential amplitude of 200 mV.

Table 2. Hardware Boot-Mode Configuration

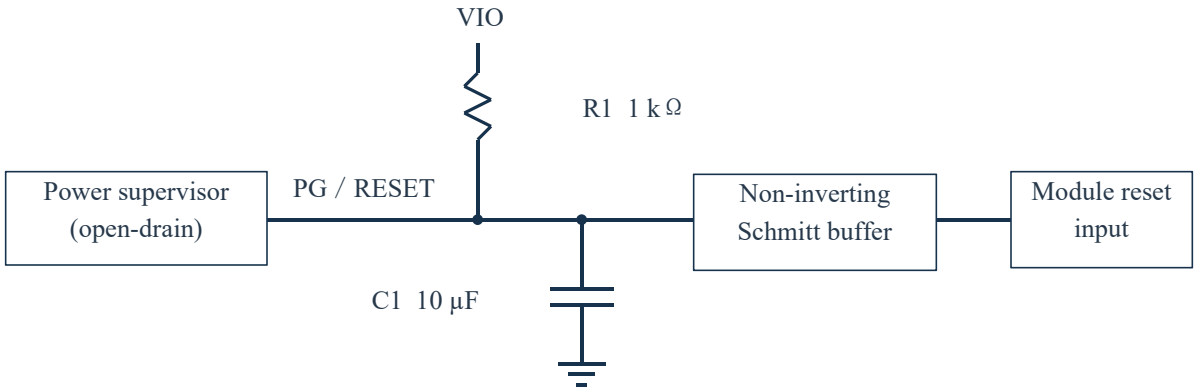
SCL	SDA	SYS_WKP	Control Mode	Data Rate Mode
0	0	Don't care	HW-forced	LDR-SE
0	1	1	HW-forced	FDR-DIFF
0	1	0	HW-forced	HDR-DIFF
1	Don't care	Don't care	I2C	Configurable via I2C

(1) LDR-SE: low-data-rate single-ended mode, 10 kbit/s–100 Mbit/s; data is carried on the SYS_WKP digital pin.

(2) FDR-DIFF: full-data-rate differential mode, 1 Mbit/s–5 Gbit/s; high-speed data is carried on SLVS differential pairs.

(3) HDR-DIFF: high-data-rate differential mode, 500 Mbit/s–6 Gbit/s; high-speed data is carried on SLVS differential pairs.

The host board may use the external RC reset circuit in Figure 7, with its output connected to CLK_FWKP. Recommended values are R1 = 1 kΩ and C1 = 10 µF, giving a nominal time constant of 10 ms. After the supply stabilizes, ensure that CLK_FWKP remains low for at least 1 ms and that the boot-strap levels are valid before releasing reset.



Select supervisor and buffer levels to suit the module interface. Connect all grounds together.

Figure 7. Recommended RC Reset Circuit

Use 8b/10b encoding for SLVS differential data at line rates above 100 Mbit/s. Before each new transmission, send an encoded, DC-balanced preamble in full before valid data. Its duration must allow link establishment and code-group synchronization. Refer to Reference Design Instructions in the companion user manual for encoding, idle and burst-timing details.

7 Electrical Characteristics

Table 3. Power and Temperature Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IN}	Input voltage	1.7	1.8	1.98	V
I_{IN}	Input current*	-	49	-	mA
P	Total power consumption	-	0.09	-	W
T_A	Operating ambient temperature	−20	-	+85	°C
T_J	Maximum junction temperature	-	-	+125	°C
T_{STG}	Storage temperature	−40	-	+105	°C

Note*: Input current of 49 mA and total power consumption of 0.09 W are typical values during 5 Gbit/s transmission/reception.

Table 4. Digital Interface, SLVS and Carrier Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IH}	High-level input voltage	1.2	1.3	-	V
V_{OH}	High-level output voltage	1.6	-	-	V
V_{IL}	Low-level input voltage	-	0.5	0.6	V
V_{OL}	Low-level output voltage	-	-	0.2	V
V_{DIFF_TX}	SLVS transmit-input differential voltage amplitude	100	200	300	mV
V_{CM_TX}	SLVS transmit-input common-mode voltage	160	-	310	mV
Z_{DIFF_TX}	Transmit-input differential impedance	-	100	-	Ω
V_{DIFF_RX}	SLVS receive-output differential voltage amplitude	80	200	300	mV
V_{CM_RX}	SLVS receive-output common-mode voltage	80	200	300	mV
Z_{DIFF_RX}	Receive-output differential impedance	-	100	-	Ω
F_{OSC}	Carrier frequency	-	60.6	-	GHz

Digital control uses 1.8 V logic; the load condition for high/low output voltages is 5 mA. The SLVS receive output uses 100 Ω differential termination, with configurable differential amplitude of 80–300 mV; 200 mV is the typical setting shown. Transmit-input common-mode voltage is 160–310 mV, and differential input amplitude is 100–300 mV.

SLVS differential voltage amplitude is the amplitude of the voltage difference between P and N; differential peak-to-peak voltage is twice this value. TXI is the transmit input from the host to the module; RXO is the receive output from the module to the host. Connect according to Table 1.

8 Assembly Instructions

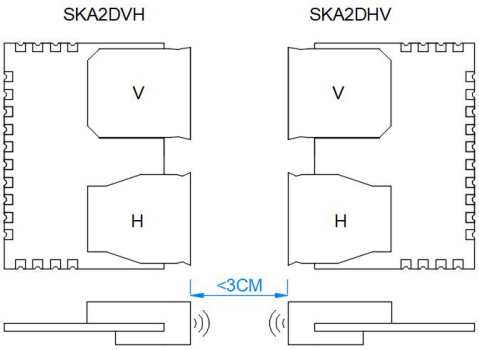


Figure 8. Paired Installation and Antenna Orientation

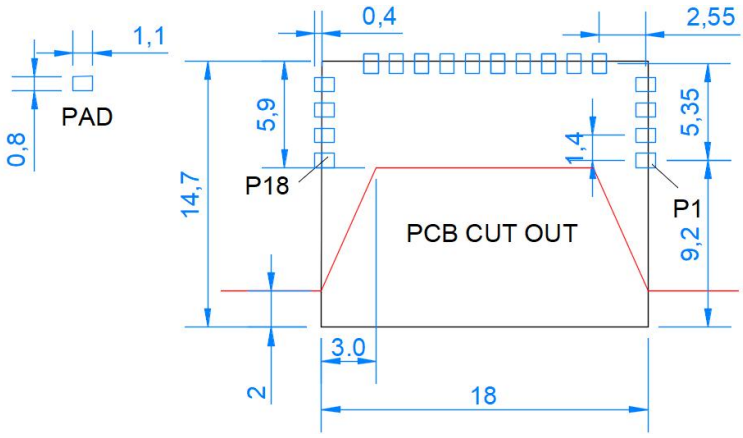


Figure 9. Host-Board Pads and Cutout Dimensions (mm)

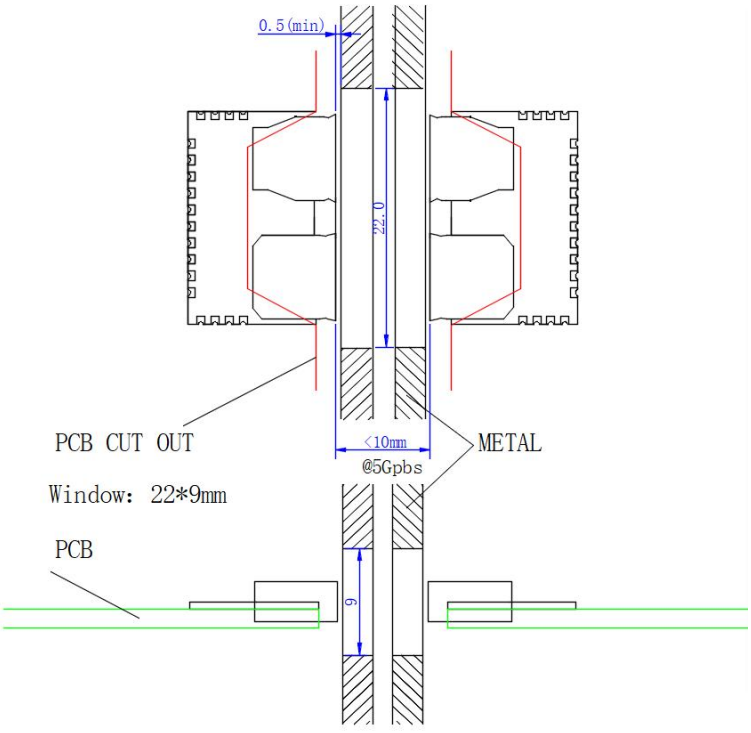


Figure 10. Metal-Housing Aperture and Module Keep-Out Area (mm)

Use Figure 9 to design the castellated pads and host-board cutout; pad size is 1.1 mm × 0.8 mm. Figure 10 shows a 22 mm × 9 mm aperture in the metal housing, with lateral clearance of at least 0.5 mm. The illustrated 5 Gbit/s installation requires an antenna gap below 10 mm.

Position and align the complementary-polarization antennas as shown in Figure 8. The recommended gap is approximately 20 mm and the mounting gap must be less than 30 mm.

Note: With a metal housing, provide a 22 mm × 9 mm nonmetallic window directly in front of the horn antennas. It may be filled with plastic or another material suitable for millimeter-wave transmission. Keep the path free of metal obstructions..

9 Product Model

Table 5. Product Models

Product Models	Description
SKA2DHV	Full-duplex castellated RF module; horizontally polarized Hantenna for reception and vertically polarized Vantenna for transmission.
SKA2DVH	Full-duplex castellated RF module; horizontally polarized Hantenna for transmission and vertically polarized Vantenna for reception.

10 Revision History

Date	Revision	Description of Changes
2019-08-05	V0.9	Initial draft.
2019-08-15	V1.0	Based on the SKA2x datasheet; removed the SKA2P1 section.
2019-08-19	V1.1	Adjusted pad dimensions.
2019-09-20	V1.2	Updated assembly apertures.
2019-11-11	V1.3	Added pictures and revised the host-board cutout.
2020-09-18	V1.4	Updated electrical characteristics.
2026-11-03	V1.5	(1) Prepared the English datasheet from the reviewed Chinese edition and organized the overview, features and applications; translated historical revision descriptions for this English edition. (2) Standardized pin definitions, hardware modes and electrical parameter names; distinguished digital-interface and SLVS quantities and normalized subscripts, positive temperatures and missing-value notation. (3) Updated reference connections, differential attenuation and the external RC reset circuit; standardized the minimum reset-low hold time to 1 ms. (4) Added module photographs and pin diagrams; organized assembly, cutout and keep-out drawings and checked captions, references and contents. (5) Standardized the bootstrap configuration table widths and layout using the SKA2Dxx user manual, retaining configuration values, pin aliases, font sizes, minimum row heights and cell margins. (6) Equalized the Min., Typ. and Max. columns in parameter tables, retaining all values, conditions, units, font sizes and standard line spacing. (7) Arranged revision history entries from oldest to newest, preserving their original dates, revisions and descriptions. (8) Checked the destinations of contents entries and section, figure and table references; rebuilt Word/WPS-compatible internal bookmark links and corrected misplaced or invalid targets. (9) Refined the product overview to integrate the chipset platform naturally into the module, antenna and functional descriptions, retaining model-specific capabilities, pairing requirements and parameters. (10) Standardized chapter names, order and content allocation using the common outline, retaining technical descriptions and illustrations; updated the contents, figure/table numbering and internal references. (11) Prepared and checked this English edition against the current Chinese edition, preserving numbered items, parameters, illustrations, commands and operating instructions.