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SK-RF CO.,Ltd

USER MANUAL

SKA2Dxx Module User Manual

60 GHz Full-Duplex Castellated RF Modules

Document Type	User Manual
Applicable Product	SKA2DHV / SKA2DVH
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Document Summary: Functions, installation and wiring, boot configuration, data tests and troubleshooting for SKA2Dxx modules, intended for hardware integration and test personnel.

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1 Functional Description

SKA2Dxx provides centimeter-scale contactless high-speed data connections between host boards. SKA2DHV and SKA2DVH form a bidirectional full-duplex link through complementary-polarization horn antennas. Each module is soldered to its local host board, accepts data from the local host and outputs data received from the opposite side.

Low-speed single-ended data is carried on SYS_WKP, while high-speed data uses TXI_P/N and RXO_P/N differential pairs. The mode is determined by boot pins at power-up or configured through I2C.

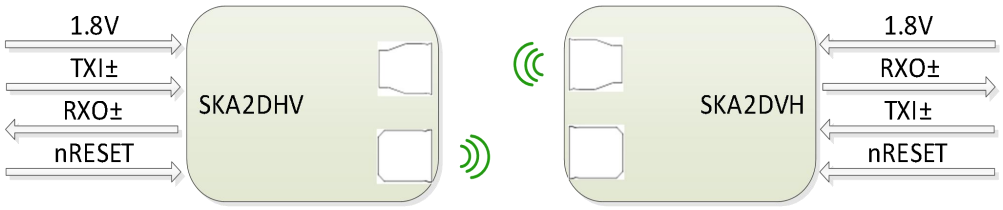


Figure 1. SKA2DHV/SKA2DVH Data Connection

2 Pin Definitions

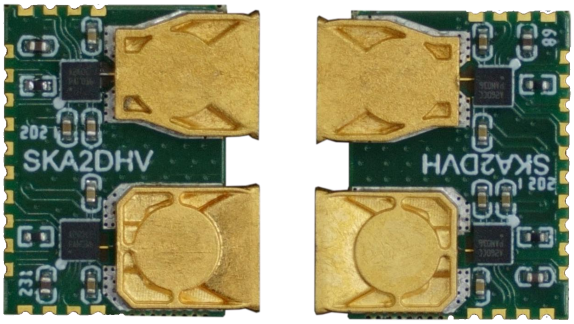


Figure 2. SKA2DHV (Left) and SKA2DVH (Right) Photographs

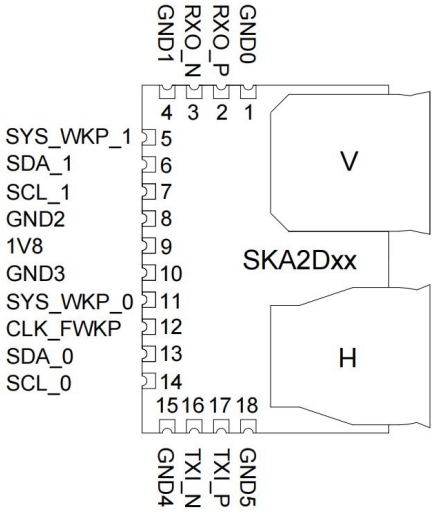


Figure 3. SKA2Dxx Pin Layout

Table 1. SKA2Dxx Pin Definitions

Pin No.	Signal Name	Description
1	GND0	Ground.
2	RXO_P	Positive differential output for wirelessly received data.
3	RXO_N	Negative differential output for wirelessly received data.
4	GND1	Ground.
5	SYS_WKP_1	Boot configuration pin; 1.8 V logic.
6	SDA_1	Boot configuration pin; 1.8 V logic.
7	SCL_1	Boot configuration pin; 1.8 V logic.
8	GND2	Ground.
9	1V8	1.8 V power input.
10	GND3	Ground.
11	SYS_WKP_0	Boot configuration pin; 1.8 V logic.
12	CLK_FWKP	Active-low reset. Keep low for at least 1 ms after the 1.8 V supply has stabilized.
13	SDA_0	Boot configuration pin; 1.8 V logic.
14	SCL_0	Boot configuration pin; 1.8 V logic.
15	GND4	Ground.
16	TXI_N	Negative differential input to the wireless transmit channel.
17	TXI_P	Positive differential input to the wireless transmit channel.
18	GND5	Ground.

3 Electrical Characteristics

Table 2. Power and Temperature Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IN}	Input voltage	1.7	1.8	1.98	V
I_{IN}	Input current*	-	49	-	mA
P	Total power consumption	-	0.09	-	W
T_A	Operating ambient temperature	−20	-	+85	°C
T_J	Maximum junction temperature	-	-	+125	°C
T_{STG}	Storage temperature	−40	-	+105	°C

Note*: Input current of 49 mA and total power consumption of 0.09 W are typical values during 5 Gbit/s transmission/reception.

Table 3. Digital Interface, SLVS and Carrier Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IH}	High-level input voltage	1.2	1.3	-	V
V_{OH}	High-level output voltage	1.6	-	-	V
V_{IL}	Low-level input voltage	-	0.5	0.6	V
V_{OL}	Low-level output voltage	-	-	0.2	V
V_{DIFF_TX}	SLVS transmit-input differential voltage amplitude	100	200	300	mV
V_{CM_TX}	SLVS transmit-input common-mode voltage	160	-	310	mV
Z_{DIFF_TX}	Transmit-input differential impedance	-	100	-	Ω
V_{DIFF_RX}	SLVS receive-output differential voltage amplitude	80	200	300	mV
V_{CM_RX}	SLVS receive-output common-mode voltage	80	200	300	mV
Z_{DIFF_RX}	Receive-output differential impedance	-	100	-	Ω
F_{OSC}	Carrier frequency	-	60.6	-	GHz

4 Reference Design

4.1 Peripheral Reference Circuit and Pin Connections

Table 4. Power and Reset Connections

Pin No.	Signal Name	Connection
9	1V8	Connect the 1.8 V supply; recommended input range: 1.7–1.98 V
1 / 4 / 8 / 10 / 15 / 18	GND0～GND5	Connect to the host-board ground plane
12	CLK_FWKP	For reset connections, see Section 4.2.

The reference circuit uses a 4.7 µF supply-decoupling capacitor. Host-board logic control uses 1.8 V levels. Check the host I/O voltage before power-up and add level translation on the host board if required.

Table 5. Data and Control Connections

Pin No.	Signal Name	Connection
17 / 16	TXI_P / TXI_N	Connect to the positive/negative differential transmit outputs of the local host
2 / 3	RXO_P / RXO_N	Connect to the positive/negative differential receive inputs of the local host
11 / 13 / 14	SYS_WKP_0 / SDA_0 / SCL_0	Group 0 boot configuration or I2C control
5 / 6 / 7	SYS_WKP_1 / SDA_1 / SCL_1	Group 1 boot configuration or I2C control

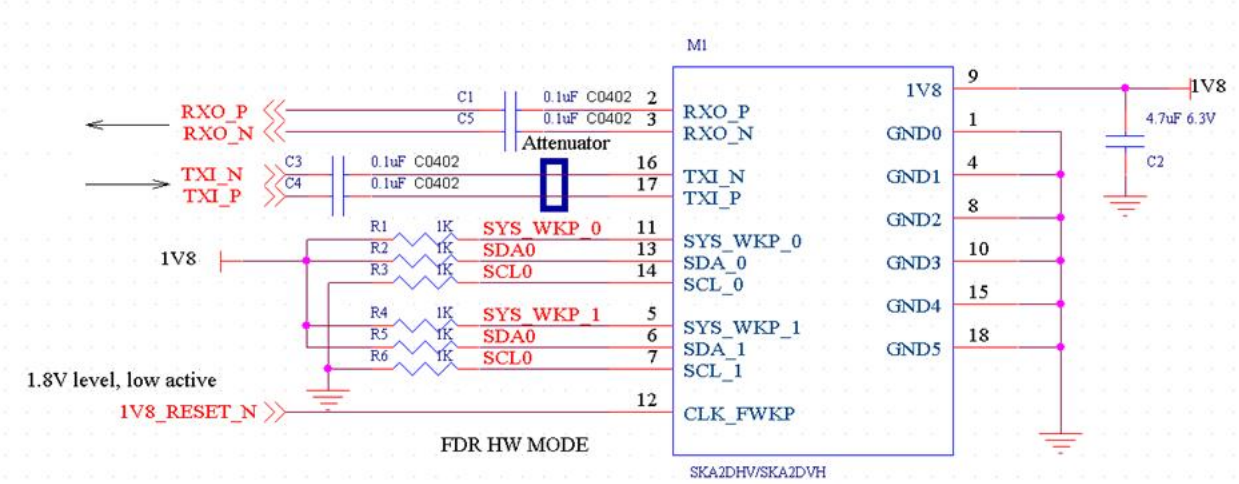
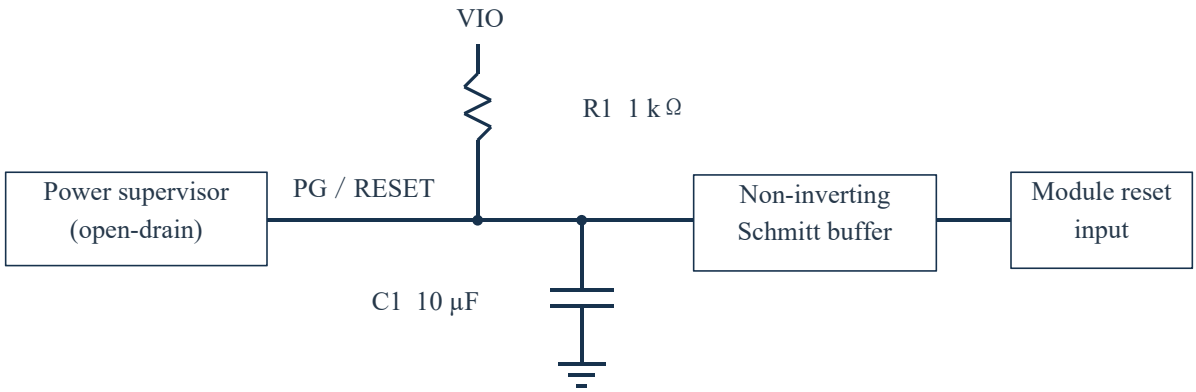


Figure 4. Module Power, Data and Boot-Configuration Reference Circuit

Route P/N as matched pairs with continuous, symmetrical differential traces. Place RXO AC-coupling capacitors near the module and TXI capacitors near the host. All illustrated capacitors are 0.1 µF, 0402.

4.2 Reset Interface

The host board may use the external RC reset circuit in Figure 5, with its output connected to CLK_FWKP. Recommended values are R1 = 1 kΩ and C1 = 10 µF, giving a nominal time constant of 10 ms. After the supply stabilizes, ensure that CLK_FWKP remains low for at least 1 ms and that the boot-strap levels are valid before releasing reset.



Select supervisor and buffer levels to suit the module interface. Connect all grounds together.

Figure 5. Recommended RC Reset Circuit

4.3 TXI Attenuation and AC Coupling

In SLVS differential mode, TXI accepts the host's differential signal. If the host output amplitude is excessive, an attenuator can bring the amplitude at the module input into the recommended range. LDR-SE uses the single-ended SYS_WKP data path and does not require this differential network.

Measure P−N differential peak-to-peak voltage at the module TXI input using the actual termination, operating rate and host output setting. The recommended input is 200–600 mVpp, equivalent to 100–300 mV differential amplitude. Within this range, use the reference connection directly. Above the upper limit, first reduce the host output setting; add attenuation if it remains excessive. Below the lower limit, check the host output setting and interconnect loss.

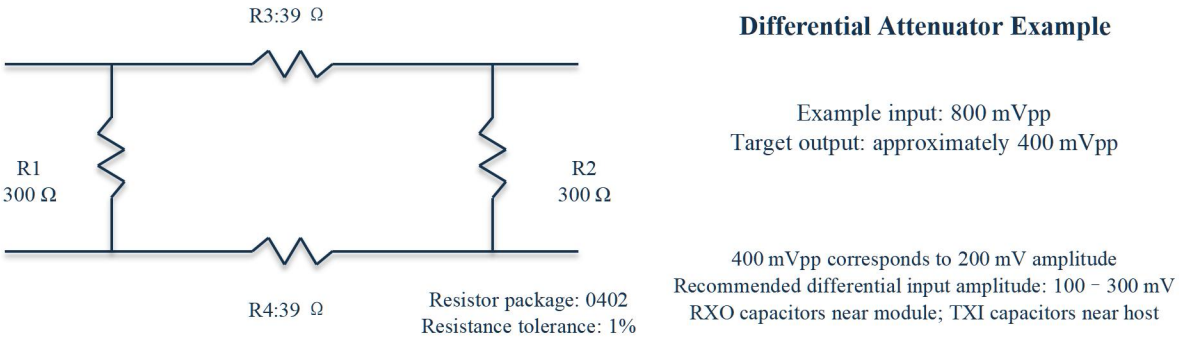


Figure 6. Differential Attenuation and AC-Coupling Example

Use Figure 6. Insert 39 Ω in series with each P and N line, and connect 300 Ω across P/N at both ends of the network. Use 0402, 1% resistors and a symmetrical layout. Place TXI AC-coupling capacitors near the host, following this model's reference circuit.

The illustrated reduction from 800 mVpp to approximately 400 mVpp is a component-selection example. After assembly, remeasure differential peak-to-peak and common-mode voltages at TXI and verify data transfer. Check this model's electrical table and adjust resistance for the actual source impedance, termination and measurements.

For a host output of 800 mV differential peak-to-peak, the 39 Ω series/300 Ω shunt 0402 network may be used to obtain approximately 400 mVpp at the module, equivalent to 200 mV differential amplitude. The receive side uses 100 Ω differential termination. Measure common-mode voltage and the P/N voltage difference separately; do not treat a single line's voltage to ground as differential amplitude.

4.4 8b/10b Data Encoding

Use 8b/10b encoding on the SLVS differential interface at line rates above 100 Mbit/s. Encoding is performed by the transmitting host, FPGA or SerDes, with corresponding decoding at the receiving host; the module carries the encoded serial signal. LDR single-ended data and differential data at or below 100 Mbit/s operate in their corresponding modes.

8b/10b maps each 8-bit data byte to a 10-bit line code group. The encoder selects valid codewords according to running disparity, maintaining DC balance and limiting consecutive identical bits to five. Sufficient transitions support receiver decisions and host clock recovery, avoiding errors caused by long runs of zeros, ones or biased data.

Use valid D code groups for data bytes and protocol-defined valid K code groups where control characters are required. The receiver checks code-group validity, running disparity and character boundaries before recovering payload data. During idle periods, send valid, DC-balanced encoded sequences and keep encoding rules consistent at both ends.

Line rate includes encoding overhead. For example, a 5 Gbit/s line provides at most 4 Gbit/s for 8b/10b data fields, before preamble, idle-character and protocol overhead. Record line rate and effective payload rate separately in host settings and test records.

64b/66b relies on scrambling for statistical DC balance and cannot directly replace the 8b/10b format required here. If the existing bus uses another encoding, adapt the format in the host or bridge logic before feeding the module's differential input.

4.5 Preamble and Burst-Data Timing

At the start of high-speed transmission, the receiver's adaptive decision threshold requires settling time. Send a continuous, DC-balanced, 8b/10b-encoded preamble before the payload, and start the application frame only after receiver decisions have stabilized. The preamble establishes the link and is not payload.

Preamble duration must cover receiver settling and code-group synchronization, with timing margin. Transmit the complete preamble before valid data begins.

Convert preamble duration to bits using the line rate: $N = \text{ceil}(R \times t_{HEADER})$. R is in bit/s and t_{HEADER} is in seconds; round up to complete 10-bit code groups. At 5 Gbit/s, 50 ns and 90 ns correspond to 250 and 450 bits. At 500 Mbit/s, they correspond to 25 and 45 bits; send at least 30 and 50 bits respectively to complete the code groups.

Choose valid 8b/10b idle or training code groups allowed by the associated protocol, maintaining continuous running disparity. The illustrated alternating 0/1 sequence explains threshold settling; actual transmission must still use valid code groups and meet receive-character alignment requirements.

If transmission stops for longer than the selected t_{HEADER}, send the complete preamble again before the next transfer. In half-duplex operation, first switch the direction at both ends and allow device states to settle, then send the preamble and finally the payload. Meet direction-switching and preamble timing separately.

The receiving host accepts application data after the preamble ends and code-group/frame boundaries are confirmed. Test initial startup, restart after long idle, direction changes, different rates and the actual assembly gap. Record discarded training data, code-group errors, disparity errors and payload verification results separately.

5 Mode Configuration

5.1 Boot Configuration

Table 6. Boot Configuration

SCL	SDA	SYS_WKP	Control Mode	Data Rate Mode
0	0	Don't care	HW-forced	LDR-SE
0	1	1	HW-forced	FDR-DIFF
0	1	0	HW-forced	HDR-DIFF
1	Don't care	Don't care	I2C	Configurable via I2C

0 and 1 denote low and high levels. Any means that the mode does not depend on that pin's value; still provide a stable level as specified by the host-board design. The two boot-pin groups correspond to the internal channels. Select matching data modes at both ends for the required transmission directions.

Table 7. Modes and Data Rates

Mode	Interface	Rate Range
LDR-SE	SYS_WKP single-ended digital interface	10 kbit/s～100 Mbit/s
FDR-DIFF	SLVS differential interface	1 Mbit/s～5 Gbit/s
HDR-DIFF	SLVS differential interface	500 Mbit/s～6 Gbit/s

(1) LDR-SE: SYS_WKP single-ended digital interface, 10 kbit/s–100 Mbit/s.

(2) FDR-DIFF: SLVS differential interface, 1 Mbit/s–5 Gbit/s.

(3) HDR-DIFF: SLVS differential interface, 500 Mbit/s–6 Gbit/s.

5.2 LDR-Mode Connection

Set SCL = 0 and SDA = 0. SYS_WKP serves as a 1.8 V single-ended data pin. Connect the two ends according to their channel directions and use this model's control interface when switching direction.

LDR boot: SCL = 0; SDA = 0; SYS_WKP carries data



Bidirectional full duplex; connect and configure each data direction separately

Figure 7. SKA2Dxx LDR Data and Boot Connections

5.3 FDR-Mode Connection

Set SCL = 0, SDA = 1 and SYS_WKP = 1. Payload data is carried on TXI/RXO differential interfaces.

FDR boot: SCL = 0; SDA = 1; SYS_WKP = 1



Bidirectional full duplex; connect and configure each data direction separately

Figure 8. SKA2Dxx FDR Data and Boot Connections

5.4 HDR-Mode Connection

Set SCL = 0, SDA = 1 and SYS_WKP = 0. Payload data is carried on TXI/RXO differential interfaces.

HDR boot: SCL = 0; SDA = 1; SYS_WKP = 0



Bidirectional full duplex; connect and configure each data direction separately

Figure 9. SKA2Dxx HDR Data and Boot Connections

6 Communication Connections

Connect each module to its local host. Connect each transmit differential input to the receive differential output at the opposite end, providing two independently connected directions that operate simultaneously. Configure both ends for the same mode and line rate.

FDR boot: SCL = 0; SDA = 1; SYS_WKP = 1



Bidirectional full duplex; connect and configure each data direction separately

Figure 10. SKA2Dxx Communication Connections

7 Assembly Instructions

7.1 Soldering and Installation Preparation

(1) Use SKA2DHV and SKA2DVH as a pair. Check model markings, pin-1 orientation and host-board pad numbering.

(2) Prepare castellated pads and PCB cutouts according to the mounting drawing. Inspect pads, vias and cutout edges before soldering.

(3) Secure and solder the modules. Check for bridged adjacent pads and power-to-ground shorts.

(4) Remove solder, metal debris and fasteners from the antenna path. Apply power only after wiring is complete.

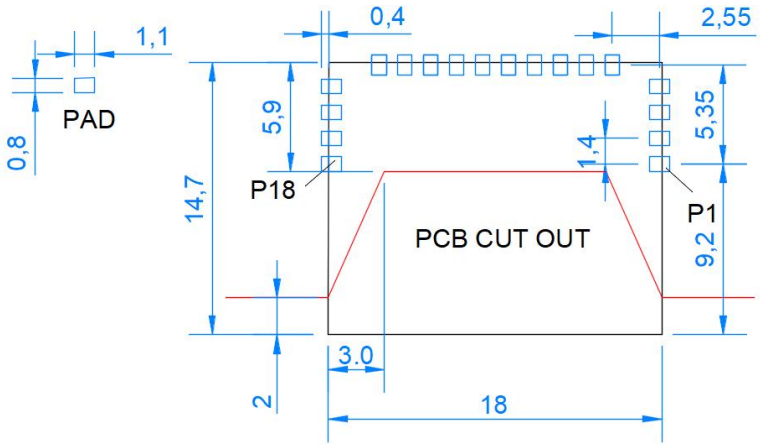


Figure 11. Host-Board Pads and Cutout Dimensions (mm)

Pad size is 1.1 mm × 0.8 mm. Follow the drawing for pad pitch and the board-cutout outline. P1 and P18 define pad-numbering references on the two sides.

7.2 Paired Assembly and Antenna Alignment

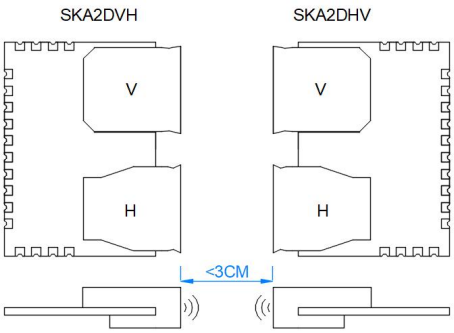


Figure 12. SKA2DHV/SKA2DVH Mounting Orientation

Face and center the horn antennas. Align horizontal-polarization channels with each other and vertical-polarization channels with each other. The recommended gap is approximately 20 mm; the mounting gap must be below 30 mm.

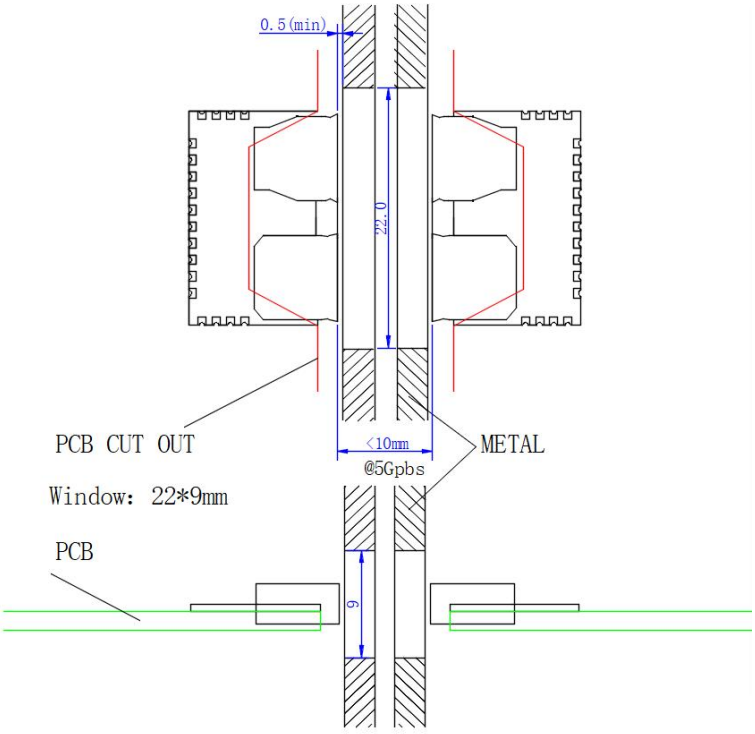


Figure 13. Metal-Housing Aperture and Keep-Out Area (mm)

For a metal housing, provide a 22 mm × 9 mm nonmetallic window directly in front of the wireless path. Illustrated lateral clearance is at least 0.5 mm. The illustrated 5 Gbit/s condition uses an antenna gap below 10 mm. The mounting structure must keep modules parallel and prevent metal from obstructing the antenna path.

Paired assembly: SKA2DHV with SKA2DVH; antenna faces opposed and aligned.

8 Power-Up and Operation

8.1 Initial Power-Up

(1) With power off, set boot levels for both SCL, SDA and SYS_WKP groups. Check the modes and host-interface rates at both ends.

(2) Hold CLK_FWKP low and apply 1.8 V power to both sides.

(3) After the supplies stabilize, keep CLK_FWKP low for at least 1 ms, then release reset.

(4) First test bidirectional data at a fixed gap with a stationary assembly, then verify the final system installation.

Before power-up, check differential input levels as described in Section 4.3. Reset connections and timing are described in Section 4.2.

9 Data Tests

9.1 Data-Transmission Tests

(1) Configure identical interface modes and compatible data rates at both hosts. Use repeatable test patterns or actual application data.

(2) Send known data from side A and verify reception at side B; then reverse direction.

(3) Enable simultaneous bidirectional transfer and record transmitted/received data volumes and error statistics for each direction.

(4) Increase the rate progressively to the target, rechecking input amplitude, termination and antenna alignment after each adjustment.

(5) Save host configuration, mode, rate, test duration, total data, errors and assembly conditions.

Where the host provides BER testing, record transmitted and erroneous bit counts. For packet data, record packet length, packet count, loss and verification errors separately.

9.2 Assembly and Reliability Tests

(1) Keep both modules fixed and repeat bidirectional tests at the target antenna gap.

(2) Install the actual housing and repeat tests with the final window material, thickness and mounting position.

(3) Check communication continuity under the displacement, vibration or motion permitted by the equipment.

(4) Test at the system's operating temperatures and save ambient temperature, gap and data statistics.

Typical module current of 49 mA and power consumption of 0.09 W apply to 5 Gbit/s transmission/reception. During testing, measure voltage at the module supply pins and record startup and operating current for host-board power design.

10 Common Questions and Operating Checks

10.1 Common Questions and Corrective Actions

Table 8. Troubleshooting

Symptom	Checks and Corrective Action
No data in either direction	Check the 1.8 V supply, common ground, CLK_FWKP reset timing, boot configuration and host data mode.
Data in one direction only	Check TXI/RXO direction, P/N polarity, both control groups and complementary-polarization models.

Symptom	Checks and Corrective Action
More errors at high rates	Check input amplitude, common-mode voltage, 100 Ω differential termination, AC-coupling capacitors and attenuation, then inspect differential routing and the antenna window.
Unstable communication inside housing	Check window dimensions, material, gap, metal obstructions and antenna alignment. Compare bare-board and assembled-system tests.

(1) Disconnect power before changing boot levels or host-board wiring. After modification, restart according to Section 8.1. Use ESD precautions when handling pads and high-speed signals. After maintenance, repeat tests in Section 9.

10.2 Technical Support

When contacting technical support, provide the product model and revision, connections and settings at both ends, power-supply conditions, indicator states, symptoms and steps to reproduce the issue. Include wiring and assembly photographs, test settings and recorded results.

11 Revision History

Date	Revision	Description of Changes
2026-11-04	V1.0	(1) Prepared the English user manual from the reviewed Chinese edition covering functions, pins, electrical characteristics, reference design, modes, connections, assembly, power-up, testing and troubleshooting. (2) Added module photographs and complete pin drawings/tables; organized power/temperature and digital-interface/SLVS/carrier parameter tables. (3) Separately described peripheral connections, the minimum 1 ms reset requirement, an external 1 kΩ/10 µF RC reset circuit, and TXI attenuation/AC coupling. (4) Added 8b/10b encoding, preamble and burst timing, with LDR/FDR/HDR boot-connection diagrams; retained I2C mode in the boot table. (5) Expanded bidirectional data tests, assembly-reliability tests and troubleshooting; retained cutout, keep-out and mounting drawings and updated figure references. (6) Equalized the Min., Typ. and Max. columns in parameter tables, retaining all values, conditions, units, font sizes and standard line spacing. (7) Checked the destinations of contents entries and section, figure and table references; rebuilt Word/WPS-compatible internal bookmark links and corrected misplaced or invalid targets. (8) Standardized chapter names, order and content allocation using the common outline, retaining technical descriptions and illustrations; updated the contents, figure/table numbering and internal references. Moved initial power-up under Power-Up and Operation, standardized Common Questions and Operating Checks, and added the information required for technical support. (9) Prepared and checked this English edition against the current Chinese edition, preserving numbered items, parameters, illustrations, commands and operating instructions.